TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/H Series

TMP95FY64

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontroller

TMP95FY64F

1. Outline and Features

The TMP95FY64F is a high-speed 16-bit microcontroller developed for use in controlling various types of middle to large-sized equipment. With 256 Kbytes of flash memory included, it allows your programs to be erased and rewritten on-board.

This device comes in a 100-pin flat package. Its features are outlined below.

(1) High-speed 16-bit CPU (900/H CPU)

- Upward compatible in instruction mnemonics with the TLCS-90 / 900
- 16 Mbytes of linear addressing space
- General-purpose registers and register bank switching
- 16-bit divide / multiply instructions and bit transfer / bitwise operation instructions
- Micro DMA: 4 channels (2 bytes in 640 ns when using a 25 MHz oscillator)

(2) Minimum instruction execution time: 160 ns (when using a 25 MHz oscillator)

(3) Internal RAM: 8 Kbytes

Internal ROM: 256-Kbyte flash memory

2-Kbyte mask ROM (used for booting)

(4) External memory extension

- Expandable up to 16 Mbytes (shared between programs and data)
- External data bus width select pin (AM8/$\overline{16}$)
- Supports coexisting 8/16-bit external data buses ..... Dynamic bus sizing

(5) 8-bit timer: 8 channels

- Event count function available (2 channels)

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
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(6) 16-bit timer / event counter: 2 channels

(7) General-purpose serial interface: 3 channels

(8) 10-bit A / D converter: 8 channels

(9) 8-bit D / A converter: 2 channels

(10) Watchdog timer

(11) Chip select / wait controller: 4 blocks

(12) Interrupt function: 45 lines of interrupt sources

- 9 CPU interrupts ..... Software interrupt instructions and undefined instruction execution
- 26 internal interrupts
- 10 external interrupts

] Seven priority levels can be set to resolve interrupt priority.

(13) Input / output port: 81 pins

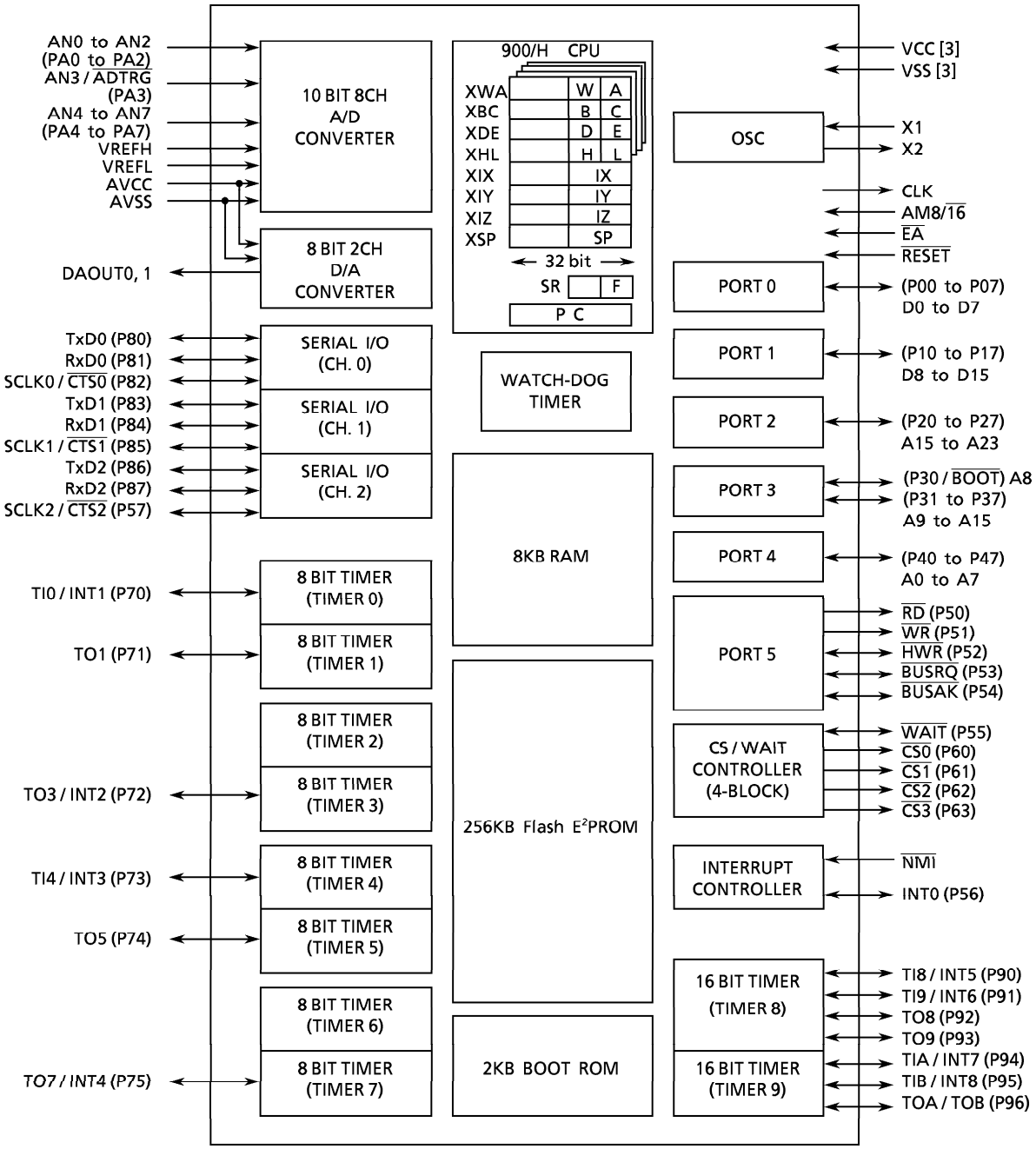
(14) Standby function

- Four halt modes (RUN, IDLE2, IDLE1, STOP)

(15) Operating voltage

- V_{CC} = 4.5 to 5.5 V

(16) Package: P-QFP100-1414-0.50E



Note: After a reset, the shared pins have their functions enclosed in ( ) selected.

Figure 1. Block Diagram of the TMP95FY64F

2. Pin Assignment and Functions

This section shows a pin assignment of the TMP95FY64F, as well as the names and the outline functions of its input / output pins.

2.1 Pin Assignment

The pin assignment of the TMP95FY64F is shown in Figure 2.1.

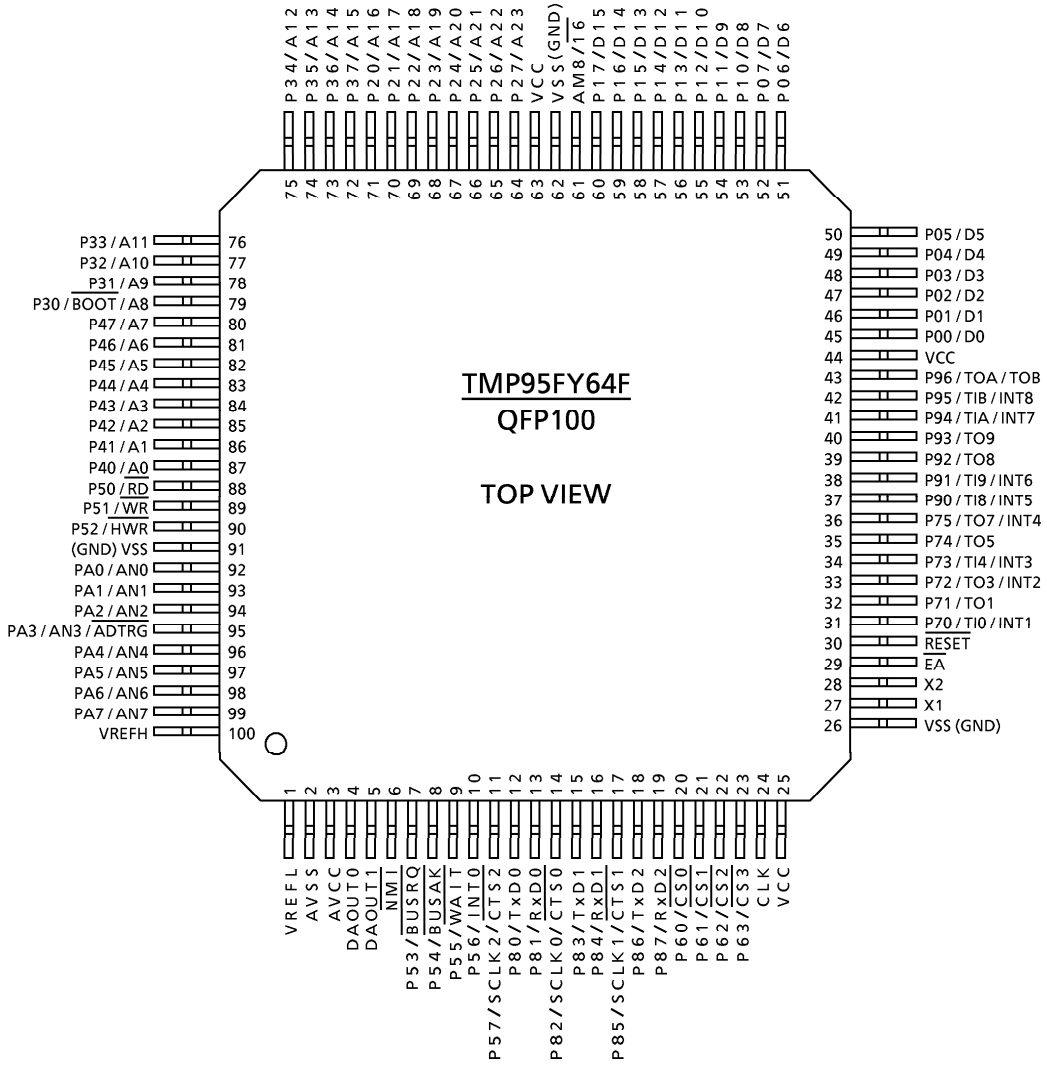


Figure 2.1 Pin Assignment of the TMP95FY64F (100-pin QFP)

2.2 Pin Names and Functions

The names and the outline functions of input / output pins are listed in Table 2.2.

Table 2.2 Pin Names and Functions (1 / 4)

Pin Name	No. of Pins	Type	Function
P00 to P07 / D0 to D7	8	Input / output	Port 0: Input / output port which can be set for input or output bit by bit.
		Input / output	Data: Data bus 0 to 7.
P10 to P17 / D8 to D15	8	Input / output	Port 1: Input / output port which can be set for input or output bit by bit.
		Input / output	Data: Data bus 8 to 15.
P20 to P27 / A16 to A23	8	Input / output	Port 2: Input / output port which can be set for input or output bit by bit.
		Output	Address: Address bus 16 to 23.
P30 / A8 / $\overline{BOOT}$	1	Input / output	Port 30: Input / output port. These pins should be pulled high with an external resistor.
		Output	Address: Address bus 8.
		Input	This pin sets single boot mode.
P31 to P37 / A9 to A15	7	Input / output	Ports 31 to 37: Input / output ports which can be set for input or output bit by bit.
		Output	Address: Address bus 9 to 15.
P40 to P47 / A0 to A7	8	Input / output	Port 4: Input / output port which can be set for input or output bit by bit.
		Output	Address: Address bus 0 to 7.
P50 / $\overline{RD}$	1	Output	Port 50: Output-only port.
		Output	Read: Strobe signal to read external memory. (The strobe signal can be output at any read timing by setting P5 <P50> = 0 and P5FC <P50F> = 1.)
P51 / $\overline{WR}$	1	Output	Port 51: Output-only port.
		Output	Write: Strobe signal to write data on pins D0 to 7.
P52 / $\overline{HWR}$	1	Input / output	Port 52: Input / output port (pull-up resistor included).
		Output	High-order write: Strobe signal to write on pins D8 to 15.
P53 / $\overline{BUSRQ}$	1	Input / output	Port 53: Input / output port (pull-up resistor included).
		Input	Bus request: Input pin to request that external bus be freed.
P54 / $\overline{BUSAK}$	1	Input / output	Port 54: Input / output port (pull-up resistor included).
		Output	Bus acknowledge: Output pin to notify that the CPU has freed external bus as requested by $\overline{BUSRQ}$.
P55 / $\overline{WAIT}$	1	Input / output	Port 55: Input / output port (pull-up resistor included).
		Input	Wait: Bus wait request to the CPU. (Effective in 1WAIT + N mode or 0 + N WAIT mode. This is set by the chip select / wait control register.)

Table 2.2 Pin Names and Functions (2 / 4)

Pin Name	No. of Pins	Type	Function
P56	1	Input / output	Port 56: Input / output port (pull-up resistor included).
/ INT0		Input	Interrupt request pin 0: Programmable (level or rising edge) interrupt request pin.
P57	1	Input / output	Port 57: Input / output port (pull-up resistor included).
/ SCLK2		Input / output	Serial clock input / output 2
/ $\overline{CTS2}$		Input	Serial data transmit ready 2 (Clear to Send)
P60	1	Output	Port 60: Output-only port.
/ $\overline{CS0}$		Output	Chip select 0: Outputs a 0 when the address is within a specified address range.
P61	1	Output	Port 61: Output-only port.
/ $\overline{CS1}$		Output	Chip select 1: Outputs a 0 when the address is within a specified address range.
P62	1	Output	Port 62: Output-only port.
/ $\overline{CS2}$		Output	Chip select 2: Outputs a 0 when the address is within a specified address range.
P63	1	Output	Port 63: Output-only port.
/ $\overline{CS3}$		Output	Chip select 3: Outputs a 0 when the address is within a specified address range.
P70	1	Input / output	Port 70: Input / output port.
/ TI0		Input	Timer input 0: Input for timer 0.
/ INT1		Input	Interrupt request pin 1: Rising edge interrupt request pin.
P71	1	Input / output	Port 71: Input / output port.
/ TO1		Output	Timer output 1: Output for timer 0 or timer 1.
P72	1	Input / output	Port 72: Input / output port.
/ TO3		Output	Timer output 3: Output for timer 2 or timer 3.
/ INT2		Input	Interrupt request pin 2: Rising edge interrupt request pin.
P73	1	Input / output	Port 73: Input / output port.
/ TI4		Input	Timer input 4: Input for timer 4.
/ INT3		Input	Interrupt request pin 3: Rising edge interrupt request pin.
P74	1	Input / output	Port 74: Input / output port.
/ TO5		Output	Timer output 5: Output for timer 4 or timer 5.
P75	1	Input / output	Port 75: Input / output port.
/ TO7		Output	Timer output 7: Output for timer 6 or timer 7.
/ INT4		Input	Interrupt request pin 4: Rising edge interrupt request pin.
P80	1	Input / output	Port 80: Input / output port (pull-up resistor included).
/ TxD0		Output	Serial transmit data 0
P81	1	Input / output	Port 81: Input / output port (pull-up resistor included).
/ RxD0		Input	Serial transmit data 0

Table 2.2 Pin Names and Functions (3 / 4)

Pin Name	No. of Pins	Type	Function
P82	1	Input / output	Port 82: Input / output port (pull-up resistor included).
/ SCLK0		Input / output	Serial clock input / output 0
/ $\overline{\text{CTS0}}$		Input	Serial data transmit ready 0 (Clear to Send).
P83	1	Input / output	Port 83: Input / output port (pull-up resistor included).
/ TxD1		Output	Serial transmit data 1
P84	1	Input / output	Port 84: Input / output port (pull-up resistor included).
/ RxD1		Input	Serial receive data 1
P85	1	Input / output	Port 85: Input / output port (pull-up resistor included).
/ SCLK1		Input / output	Serial clock input / output 1
/ $\overline{\text{CTS1}}$		Input	Serial data transmit ready 1 (Clear to Send)
P86	1	Input / output	Port 86: Input / output port (pull-up resistor included).
/ TxD2		Output	Serial transmit data 2
P87	1	Input / output	Port 87: Input / output port (pull-up resistor included).
/ RxD2		Input	Serial receive data 2
P90	1	Input / output	Port 90: Input / output port.
/ TI8		Input	Timer input 8: Input pin for timer 8
/ INT5		Input	Interrupt request pin 5: Programmable (rising or falling edge) interrupt request pin.
P91	1	Input / output	Port 91: Input / output port.
/ TI9		Input	Timer input 9: Input pin for timer 8
/ INT6		Input	Interrupt request pin 6: Rising edge interrupt request pin.
P92	1	Input / output	Port 92: Input / output port.
/ TO8		Output	Timer output 8: Output pin for timer 8
P93	1	Input / output	Port 93: Input / output port.
/ TO9		Output	Timer output 9: Output pin for timer 8
P94	1	Input / output	Port 94: Input / output port.
/ TIA		Input	Timer input A: Input pin for timer 9
/ INT7		Input	Interrupt request pin 7: Programmable (rising or falling edge) interrupt request pin.
P95	1	Input / output	Port 95: Input / output port.
/ TIB		Input	Timer input B: Input pin for timer 9
/ INT8		Input	Interrupt request pin 8: Rising edge interrupt request pin.
P96	1	Input / output	Port 96: Input / output port.
/ TOA		Output	Timer output A: Output pin for timer 9
/ TOB		Output	Timer output B: Output pin for timer 9
PA0 to PA2	3	Input	Port A0 to A2: Input-only port.
/ AN0 to AN2		Input	Analog input 2 to 0: Input pin for the A / D converter.

Table 2.2 Pin Names and Functions (4 / 4)

Pin Name	No. of Pins	Type	Function
PA3	1	Input	Port A3: Input-only port.
/ AN3		Input	Analog input 3: Input pin for the A / D converter.
/ $\overline{\text{ADTRG}}$		Input	External start trigger
PA4 to PA7	4	Input	Port A4 to A7: Input-only port.
/ AN4 to AN7		Input	Analog input 4 to 7: Input pin for the A / D converter.
DAOUT0	1	Output	D / A output 0: Output pin of D / A converter 0.
DAOUT1	1	Output	D / A output 1: Output pin of D / A converter 1.
$\overline{\text{NMI}}$	1	Input	Nonmaskable interrupt request pin: Programmable (rising edge or rising / falling edges) interrupt request pin.
CLK	1	Output	Clock output: Clock derived from an external clock by dividing it by 4. This output is pulled high during a reset.
$\overline{\text{EA}}$	1	Input	External access: Connect this pin to Vcc.
AM8 / $\overline{16}$	1	Input	Address mode: External data bus width select pin. Connect this pin to Vcc. The external data bus width to be accessed can be set by the chip select / wait control register.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes the TMP95FY64. (Pull-up resistor included.)
VREFH	1	Input	Reference voltage input pin (H) for the A / D converter.
VREFL	1	Input	Reference voltage input pin (L) for the A / D converter.
AVCC	1		Power supply pin as well as the reference voltage input pin for the A / D converter. (Be sure to connect this pin to the power supply rail.)
AVSS	1		GND pin as well as the reference voltage input pin for the A / D converter. (Be sure to connect this pin to GND.)
X1 / X2	2	Input / Output	Oscillator connecting pin.
VCC	3		Power supply pin: Connect all VCC pins to the power supply rail.
VSS	3		GND pin: Connect all VSS pins to GND (0 V).

Note: All pins with pull-up resistors included, except the $\overline{\text{RESET}}$ pin, can have their pull-up resistors electrically isolated from the pin by software.

3. Functional Description

This section shows the hardware configuration of the TMP95FY64 and explains how it operates.

This device is a version of the created by replacing the predecessor's internal mask ROM with a 256-Kbyte internal flash memory and expanding its internal RAM size to 8 Kbytes. The configuration and the functionality of this device are the same as those of the TMP95CS64. For the functions of this device that are not described here, refer to the TMP95CS64 data sheet.

3.1 Outline of Operation Modes

There are single-chip and single-boot modes. Which mode is selected depends on the device's pin state after a reset.

- Single-chip mode: The device normally operates in this mode. After a reset, the device starts executing the internal flash memory program.
- Single-boot mode: This mode is used to rewrite the internal flash memory by serial transfer (UART). After a reset, the internal boot ROM starts up, executing a on-board rewrite program.

Table 3.1 (1) Operation Mode Setup Table

Operation Mode	Mode Setup Input Pin		
	$\overline{\text{RESET}}$	$\overline{\text{BOOT}}$	$\overline{\text{EA}}$
Single-chip mode	↑	1	1
Single-boot mode		0	1

Note: The $\overline{\text{BOOT}}$ pin (P30) should be pulled high with an external resistor.

3.2 Memory Map

The memory map of this device differs from that of the TMP95CS64.

Figure 3.2 shows a memory map of the device in single-chip mode and its memory areas that can be accessed in each addressing mode of the CPU.

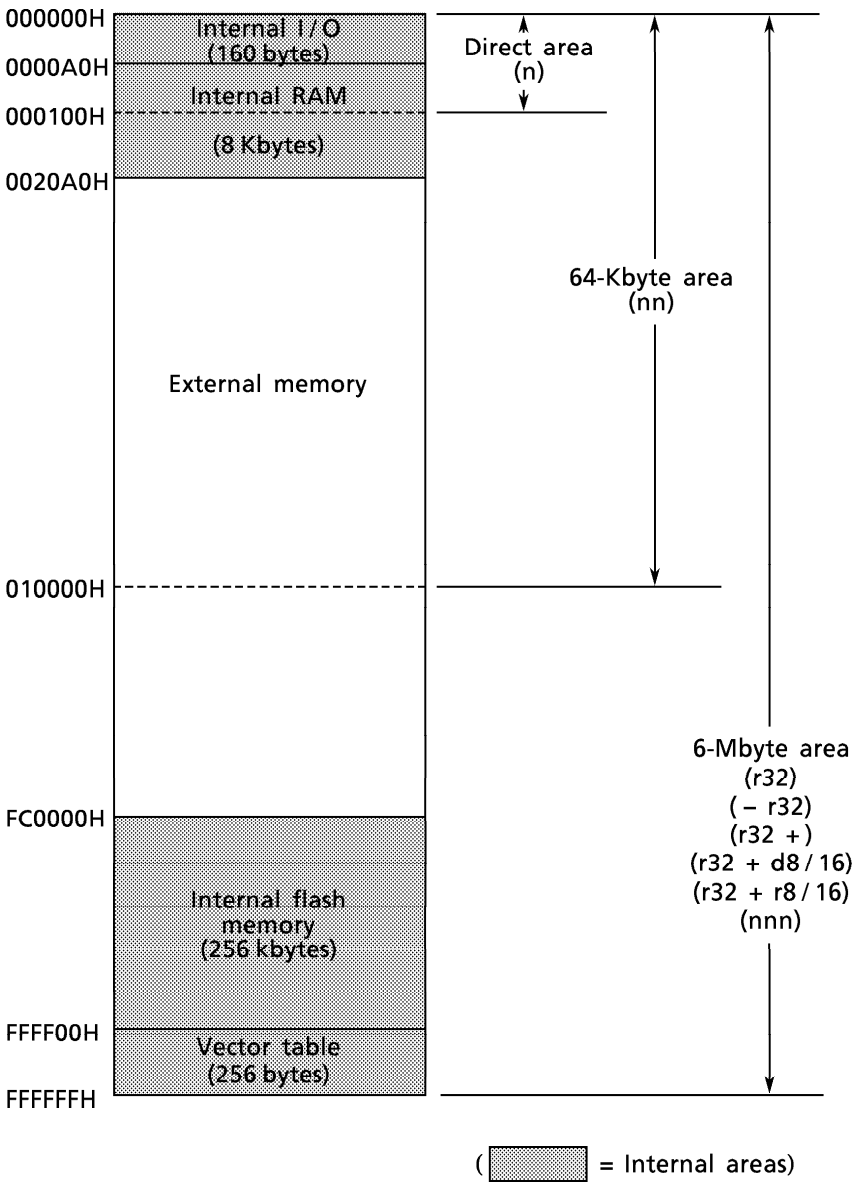


Figure 3.2 Memory Map of the TMP95FY64 (Single-chip Mode)

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 6.5	V
Input Voltage	V_{IN}	− 0.5 to V_{CC} + 0.5	V
Output Current (Total)	ΣI_{OL}	+ 120	mA
Output Current (Total)	ΣI_{OH}	− 120	mA
Power Dissipation (Ta = + 70°C)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	+ 260	°C
Storage Temperature	T_{STG}	− 65 to + 150	°C
Operating Temperature	T_{OPR}	− 20 to + 70	°C
Number of Times Program Erased	N_{EW}	1000	Cycle

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics

(1) V_{CC} = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

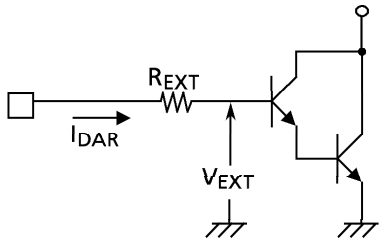
(Single-chip mode, single-boot mode)

Parameter	Symbol	Test Condition	Min	Max	Unit
Low Level Input Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75) RESET, NMI, INT0 to 4 EA, AM8 / 16 X1	V_{IL} V_{IL1} V_{IL2} V_{IL3} V_{IL4}	—	− 0.3 − 0.3 − 0.3 − 0.3 − 0.3	0.8 0.3 V_{CC} 0.25 V_{CC} 0.3 0.2V_{CC}	V V V V V
High Level Input Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75) RESET, NMI, INT0 to 4 EA, AM8 / 16 X1	V_{IH} V_{IH1} V_{IH2} V_{IH3} V_{IH4}	—	2.2 0.7 V_{CC} 0.75 V_{CC} V_{CC} − 0.3 0.8V_{CC}	V_{CC} + 0.3 V_{CC} + 0.3 V_{CC} + 0.3 V_{CC} + 0.3 V_{CC} + 0.3	V V V V V
Low Level Output Voltage	V_{OL}	I_{OL} = 1.6 mA		0.45	V
High Level Output Voltage	V_{OH} V_{OH1} V_{OH2}	I_{OH} = − 400 μA I_{OH} = − 100 μA I_{OH} = − 20 μA	2.4 0.75 V_{CC} 0.9 V_{CC}	—	V V V
Output Port Current (8 output pins max.)	I_{DAR}	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ	− 1.0	− 3.5	mA
Input Leakage Current Output Leakage Current	I_{LI} I_{LO}	0.0 ≦ Vin ≦ V_{CC} 0.2 ≦ Vin ≦ V_{CC} − 0.2	0.02 (Typ.) 0.05 (Typ.)	± 5 ± 10	μA μA
Operating Current (RUN) IDLE2 IDLE1 STOP (Ta = − 20 to + 70°C)	I_{CC}	fc = 25 MHz 0.2 ≦ Vin ≦ V_{CC} − 0.2		100 40 10 150	mA mA mA μA
Power-down Voltage (@STOP, RAM backup)	V_{STOP}	V_{IL2} = 0.2 V_{CC}, V_{IH2} = 0.8 V_{CC}	2.0	6.0	V
Pull-up Resistance	R_{RP}		45	160	kΩ
Pin Capacitance	C_{IO}	fc = 1 MHz	—	10	pF
Schmitt Width RESET, NMI, INT0 to 4	V_{TH}		0.4	1.0 (Typ.)	V

Note 1: The Typ. values are referenced to V_{CC} = + 5 V at Ta = + 25°C.

Note 2: The I_{DAR} stipulated above is guaranteed for a total of 8 lines of any output ports used.

Reference diagram: Definition of I_{DAR}



4.3 AC Characteristics

(1) V_{CC} = + 5 V ± 10%, Ta = − 20 to + 70°C

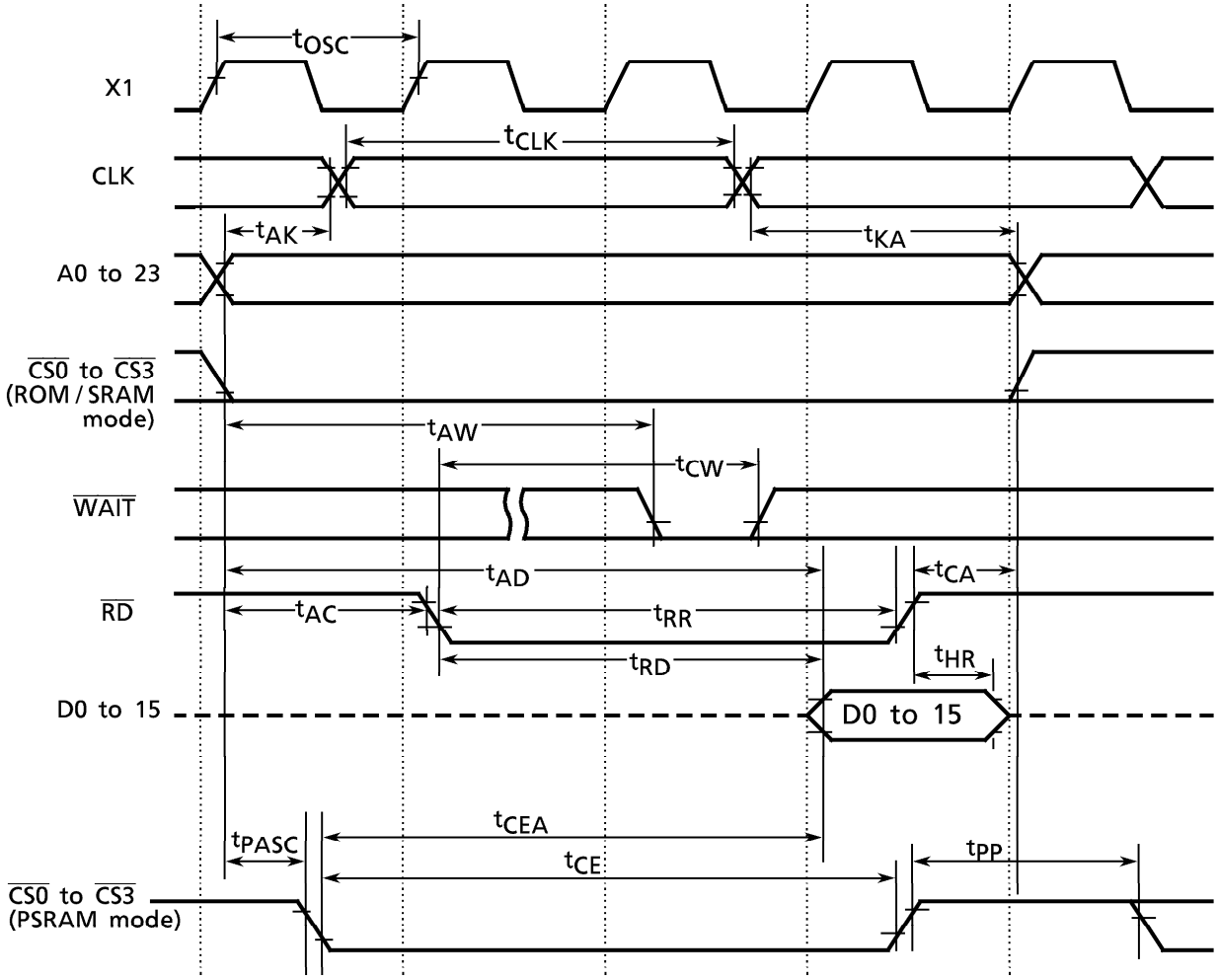
(fc = 8 MHz to 25 MHz)

No.	Parameter	Sym-bol	Variable		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Oscillation Period (= x)	t_{OSC}	40	125	50	—	40	—	ns
2	CLK Pulse Width	t_{CLK}	2.0x − 40	22.5	60	—	40	—	ns
3	Valid A0 to 23 → CLK hold	t_{AK}	0.5x − 20	0	5	—	0	—	ns
4	Valid CLK → A0 to 23 hold	t_{KA}	1.5x − 60	0	15	—	0	—	ns
5	Valid A0 to 23 → $\overline{RD}$ / $\overline{WR}$ fall	t_{AC}	1.0x − 20	11.25	30	—	20	—	ns
6	$\overline{RD}$ / $\overline{WR}$ rise → A0 to 23 hold	t_{CA}	0.5x − 20	5	5	—	0	—	ns
7	Valid A0 to 23 → D0 to 15 input	t_{AD}	69.4	3.5x − 40	—	135	—	100	ns
8	$\overline{RD}$ fall → D0 to 15 input	t_{RD}	33.1	2.5x − 45	—	80	—	55	ns
9	$\overline{RD}$ low pulse width	t_{RR}	2.5x − 40	38.1	85	—	60	—	ns
10	$\overline{RD}$ rise → D0 to 15 hold	t_{HR}	0	0	0	—	0	—	ns
11	$\overline{WR}$ low pulse width	t_{WW}	2.5x − 40	38.1	85	—	60	—	ns
12	Valid D0 to 15 → $\overline{WR}$ rise	t_{DW}	2.0x − 40	22.5	60	—	40	—	ns
13	$\overline{WR}$ rise → D0 to 15 hold	t_{WD}	0.5x − 10	5.6	15	—	10	—	ns
14	Valid A0 to 23 → $\overline{WAIT}$ input (1 WAIT + n mode)	t_{AW}	19.4	3.5x − 90	—	85	—	50	ns
	Valid A0 to 23 → $\overline{WAIT}$ input (0 + n WAIT mode)	t_{AW}	6.8	1.5x − 40	—	35	—	20	ns
15	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold (1 WAIT + n mode)	t_{CW}	2.5x + 0	78.1	125	—	100	—	ns
	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold (0 + n WAIT mode)	t_{CW}	0.5x + 0	15.6	25	—	20	—	ns
16	$\overline{WR}$ rise → valid PORT	t_{CP}	—	200	—	200	—	200	ns
17	$\overline{CS}$ low pulse width (PSRAM mode)	t_{CE}	3.0x − 40	—	110	—	80	—	ns
18	$\overline{CS}$ fall → D0 to 15 input (SRAM mode)	t_{CEA}	—	3.0x − 60	—	90	—	60	ns
19	Address setup time (SRAM mode)	t_{PASC}	0.5x − 15	—	10	—	5	—	ns
20	$\overline{CS}$ precharge time (SRAM mode)	t_{PP}	1.0x − 10	—	40	—	30	—	ns

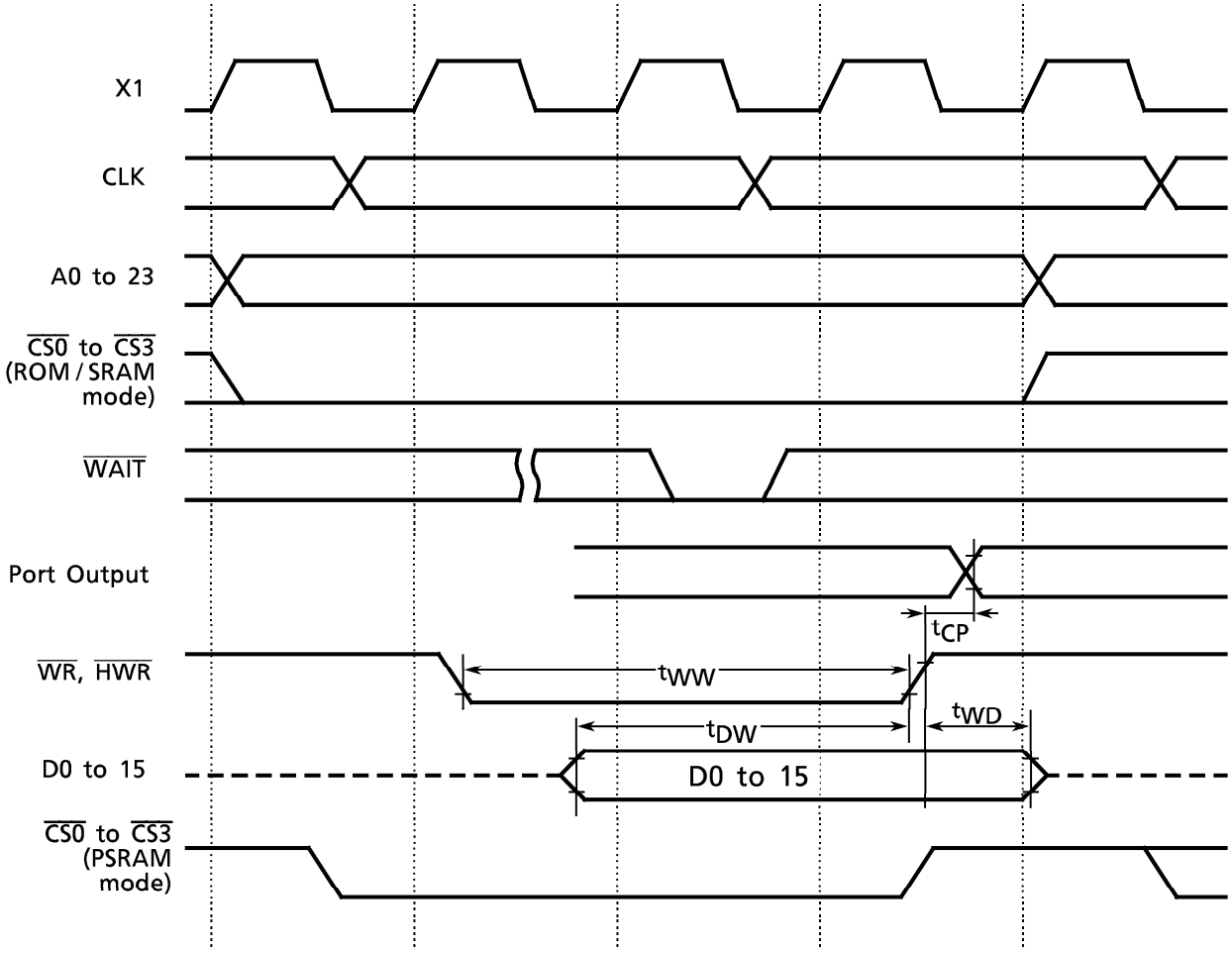
AC test conditions

- Output level: High 2.2 V / Low 0.8 V, CL = 50 pF
- Input level: High 2.4 V / Low 0.45 V (D0 to D15)
  High 0.8 V_{CC} / Low 0.2 Vcc (except for D0 to D15)

(2) Read cycle


tOSC
X1
tCLK
CLK
tAK
tKA
A0 to 23
CS0 to CS3
(ROM / SRAM
mode)
tAW
tCW
WAIT
tAD
tCA
RD
tAC
tRR
tRD
tHR
D0 to 15
D0 to 15
tCEA
tPASC
tCE
tPP
CS0 to CS3
(PSRAM mode)

(3) Write cycle



4.4 Serial Channel Timing

(1) I/O interface modes

① SCLK input mode

V_{CC} = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

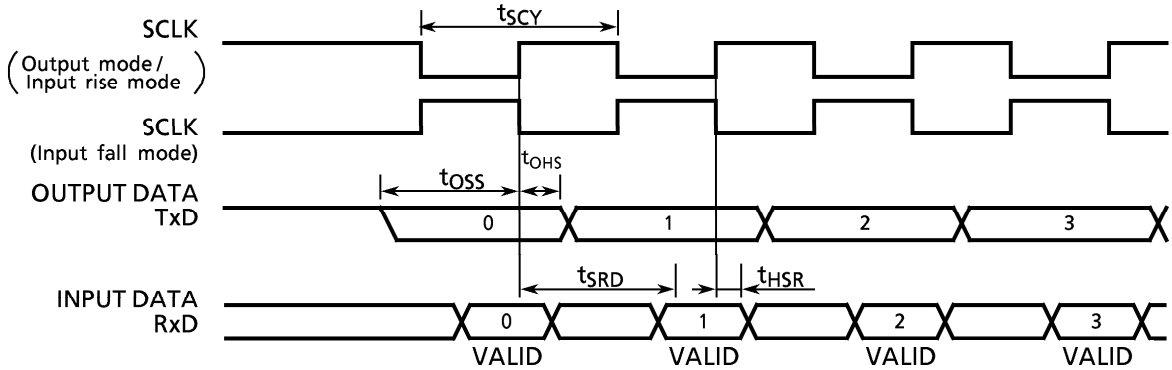
Parameter	Symbol	Variable		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK period	t_{SCY}	16x	—	1.6	—	0.64	—	μs
Output data → SCLK rise / fall*	t_{OSS}	t_{SCY} / 2 − 5x − 50	—	250	—	70	—	ns
SCLK rise / fall* → Output data hold	t_{OHS}	5x − 100	—	400	—	100	—	ns
SCLK rise / fall* → Input data hold	t_{HSR}	0	—	0	—	0	—	ns
SCLK rise / fall* → Valid data input	t_{SRD}	—	t_{SCY} − 5x − 100	—	1000	—	340	ns

*) SCLK rise / fall refers to the timing at which SCLK rises when in SCLK rising edge mode or at which SCLK falls when in SCLK falling edge mode.

② SCLK output mode

V_{CC} = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Variable		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK period (programmable)	t_{SCY}	16x	8192x	1.6	819.2	0.64	327.6	μs
Output data → SCLK rise	t_{OSS}	t_{SCY} − 2x − 150	—	1250	—	410	—	ns
SCLK rise → Output data hold	t_{OHS}	2x − 80	—	120	—	0	—	ns
SCLK rise → Input data hold	t_{HSR}	0	—	0	—	0	—	ns
SCLK rise → Valid data input	t_{SRD}	—	t_{SCY} − 2x − 150	—	1250	—	410	ns



(2) UART mode (SCLK0 to 2 external inputs)

V_{CC} = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Variable		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Period	t_{SCY}	4x + 20	—	420	—	180	—	ns
SCLK Low Level Pulse Width	t_{SCYL}	2x + 5	—	205	—	85	—	ns
SCLK High Level Pulse Width	t_{SCYH}	2x + 5	—	205	—	85	—	ns

4.5 A / D Conversion Characteristics

V_{CC} = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

Parameter		Sym-bol	Min	Typ.	Max	Unit
A / D Analog Reference Supply Voltage (+)		V_{REFH}	V_{CC} − 0.2	—	V_{CC}	V
A / D Analog Reference Supply Voltage (−)		V_{REFL}	V_{SS}	—	V_{SS} + 0.2	
Analog Reference Voltage		AV_{CC}	V_{CC} − 0.2	—	V_{CC}	
Analog Reference Voltage		AV_{SS}	V_{SS}	—	V_{SS} + 0.2	
Analog Input Voltage		V_{AIN}	V_{REFL}	—	V_{REFH}	
Analog Reference Voltage Power Supply Current	<VREFON> = 1	I_{REF}	—	—	3.7	mA
	<VREFON> = 0		—	0.02	5.0	μA
Overall Error (Not Including Quantization Error)		E_T	—	± 1	± 3	LSB

Note 1: $1LSB = (VREFH - VREFL) / 2^{10}$ [V]

Note 2: The power supply current flowing from the AV_{CC} pin is included in the power supply current I_{CC} of the V_{CC} pin.

4.6 D / A Conversion Characteristics

V_{CC} = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	AV_{CC}	—	V_{CC} − 0.2	—	V_{CC}	V
Analog Reference Voltage	AV_{SS}		V_{SS}	—	V_{SS} + 0.2	
Overall Error	—	R = 1 MΩ (Note) R = 5 MΩ (Note) R = 10 MΩ (Note)	—	—	7.0 4.0 3.5	LSB LSB LSB
Differential Linearity Error		—	—	2.0	—	LSB

Note: R denotes the external load resistance of D / A converter output pins (DAOUT0, DAOUT1).

4.7 Event Counter (External Input Clocks: TI0, TI4, TI8, TI9, TIA, TIB)

V_{CC} = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Variable		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
External Input Clock Period	t_{VCK}	8x + 100	—	900	—	420	—	ns
External Input Clock Low Level Pulse Width	t_{VCKL}	4x + 40	—	440	—	200	—	ns
External Input Clock High Level Pulse Width	t_{VCKH}	4x + 40	—	440	—	200	—	ns

4.8 Interrupt Operation

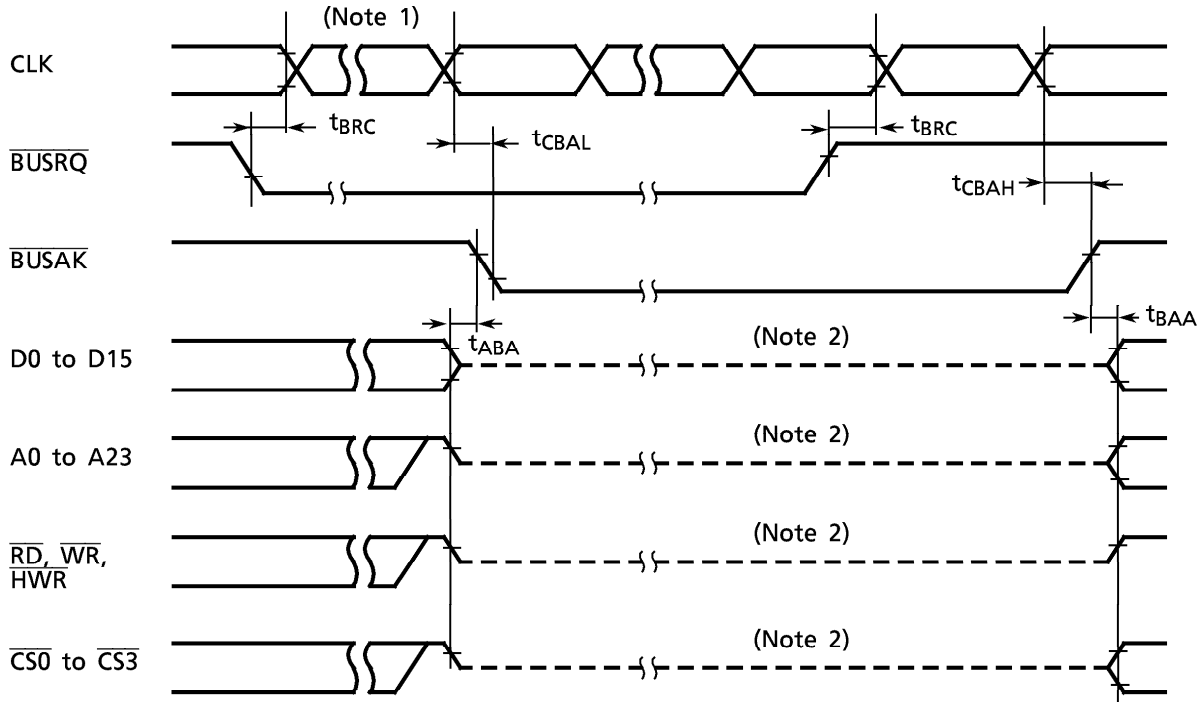
V_{CC} = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Variable		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$ and INT0 to 4 Low Level Pulse Width	t_{INTAL}	4x	—	400	—	160	—	ns
$\overline{NMI}$ and INT0 to 4 High Level Pulse Width	t_{INTAH}	4x	—	400	—	160	—	ns
INT5 to INT8 Low Level Pulse Width	t_{INTBL}	8x + 100	—	900	—	420	—	ns
INT5 to INT8 High Level Pulse Width	t_{INTBH}	8x + 100	—	900	—	420	—	ns

4.9 Bus Request / Bus Acknowledge Timing

V_{CC} = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Variable		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ setup time relative to CLK	t_{BRC}	120	—	120	—	120	—	ns
CLK→$\overline{BUSAK}$ fall	t_{CBAL}	—	2.0x + 120	—	320	—	200	ns
CLK→$\overline{BUSAK}$ rise	t_{CBAH}	—	0.5x + 40	—	90	—	60	ns
Duration from output buffer turn-off to $\overline{BUSAK}$ fall	t_{ABA}	0	80	0	80	0	80	ns
Duration from $\overline{BUSAK}$ rise to output buffer turn-on	t_{BAA}	0	80	0	80	0	80	ns



Note 1: If when control of the bus is requested by pulling $\overline{BUSRQ}$ low, the preceding bus cycle is not completed due to wait state, the bus will not be relinquished until exiting from the wait state.

Note 2: The broken line only indicates that the output buffer is turned off, and not that the signal is at an intermediate voltage level. Immediately after the bus is relinquished, the immediately preceding signal level is dynamically held on by an external load capacitance. Therefore, if the signal level needs to be set high or low using an external resistor, the signal level setup immediately after relinquishing the bus may be delayed by the external load capacitance (RC time constant). Consider this delay when designing your system. The built-in programmable pullup resistors continue working depending on the internal signal state.