

# TP3076 COMBO<sup>®</sup> II Programmable PCM CODEC/Filter for ISDN and Digital Phone Applications

Check for Samples: [TP3076](#)

## FEATURES

- Complete CODEC and Filter system including:
  - Transmit and receive PCM channel filters
  - $\mu$ -law or A-law companding coder and decoder
  - Receive power amplifier drives 300 $\Omega$
  - 4.096 MHz serial PCM data (max)
- Programmable functions:
  - Transmit gain: 25.4 dB range, 0.1 dB steps
  - Receive gain: 25.4 dB range, 0.1 dB steps
  - Time-slot assignment; to 64 slots/frame
- 4 interface latches
- A or  $\mu$ -law
- Analog loopback
- Digital loopback
- Direct interface to solid-state SLICs
- Standard serial control interface
- 80 mW operating power (typ)
- 1.5 mW standby power (typ)
- Designed for CCITT and LSSGR specifications
- TTL and CMOS compatible digital interfaces

## DESCRIPTION

The TP3076 is a second-generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber line and trunk cards and digital phone applications. Using advanced switched capacitor techniques, COMBO II combines transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and  $\mu$ -law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

Channel gains are programmable over a 25.4 dB range in each direction.

To enable COMBO II to interface to the SLIC control leads, a number of programmable latches are included; each may be configured as either an input or an output. The TP3076 provides 4 latches.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## NOTE

See also AN-614 COMBO II application guide.

## Absolute Maximum Ratings <sup>(1)</sup>

$V_{CC}$ to GND	7V
Voltage at $V_{F_XI}$	$V_{CC} + 0.5V$ to $V_{BB} - 0.5V$
Voltage at Any Digital Input	$V_{CC} + 0.5V$ to GND $- 0.5V$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
$V_{BB}$ to GND	$-7V$
Current at $V_{F_R0}$	$\pm 100$ mA
Current at Any Digital Output	$\pm 50$ mA
Lead Temperature (Soldering, 10 sec.)	$300^{\circ}C$

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.



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## Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ . All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typical values specified at  $V_{CC} = +5V$ ,  $V_{BB} = -5V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DIGITAL INTERFACES</b>						
$V_{IL}$	Input Low Voltage <sup>(1)</sup>	All Digital Inputs (DC Meas.)			<b>0.7</b>	V
$V_{IH}$	Input High Voltage <sup>(1)</sup>	All Digital Inputs (DC Meas.) <sup>(2)</sup>	<b>2.0</b>			V
$V_{OL}$	Output Low Voltage	$D_X1$ , $\overline{TS}_X1$ , and CO, $I_L = 3.2$ mA, All Other Digital Outputs, $I_L = 1$ mA			<b>0.4</b>	V
$V_{OH}$	Output High Voltage	$D_X1$ and CO, $I_L = -3.2$ mA, All Other Digital Outputs (except $\overline{TS}_X$ ), $I_L = -1$ mA All Digital Outputs, $I_L = -100$ $\mu$ A	<b>2.4</b>			V
			$V_{CC} - 0.5$			V
$I_{IL}$	Input Low Current	Any Digital Input, $GND < V_{IN} < V_{IL}$	<b>-10</b>		<b>10</b>	$\mu$ A
$I_{IH}$	Input High Current	Any Digital Input, except MR, $V_{IH} < V_{IN} < V_{CC}$ MR Only	<b>-10</b>		<b>100</b>	$\mu$ A
$I_{OZ}$	Output Current in High Impedance State ( TRI-STATE <sup>®</sup> )	$D_X1$ , $\overline{TS}_X1$ and CO IL3–IL0 when Selected as Inputs $GND < V_{OUT} < V_{CC}$	<b>-10</b>		<b>10</b>	$\mu$ A
<b>ANALOG INTERFACES</b>						
$I_{VFXI}$	Input Current, $V_{FXI}$	$-3.3V < V_{FXI} < 3.3V$	<b>-1.0</b>		<b>1.0</b>	$\mu$ A
$R_{VFXI}$	Input Resistance	$-3.3V < V_{FXI} < 3.3V$	<b>1.0</b>			M $\Omega$
$VOS_X$	Input Offset Voltage	Transmit Gain = 0 dB Applied at $V_{FXI}$			200 10	mV mV
$RL_{VFRO}$	Load Resistance	Receive Gain = 0 dB Receive Gain = -0.5 dB Receive Gain = -1.2 dB	15k 600 <b>300</b>			$\Omega$
$CL_{VFRO}$	Load Capacitance	$RL_{VFRO} \geq 300\Omega$ $CL_{VFRO}$ from $V_{FRO}$ to GND			<b>200</b>	pF
$RO_{VFRO}$	Output Resistance	Steady Zero PCM Code Applied to $D_R1$		1.0	3.0	$\Omega$
$VOS_R$	Output Offset Voltage	Alternating $\pm$ Zero PCM Code Applied at $V_{FRO}$ $D_R1$ , Maximum Receive Gain	<b>-200</b>		<b>200</b>	mV
<b>POWER DISSIPATION</b>						
$I_{CC0}$	Power Down Current	CCLK, CI, CO = 0.4V, $\overline{CS} = 2.4V$ Interface Latches Set as Outputs with No Load, All Other Inputs Active, Power Amp Disabled		0.1	<b>0.6</b>	mA
$I_{BB0}$	Power Down Current	As Above		-0.1	<b>-0.3</b>	mA
$I_{CC1}$	Power Up Current	CCLK, CI, CO = 0.4V, $\overline{CS} = 2.4V$ No Load on Power Amp Interface Latches Set as Outputs with No Load		8.0	<b>11.0</b>	mA
$I_{BB1}$	Power Up Current	As Above		-8.0	<b>-11.0</b>	mA
$I_{CC2}$	Power Down Current	As Above, Power Amp Enabled		2.0	<b>3.0</b>	mA
$I_{BB2}$	Power Down Current	As Above, Power Amp Enabled		-2.0	<b>-3.0</b>	mA

- (1) A signal is Valid if it is above  $V_{IH}$  or below  $V_{IL}$  and Invalid if it is between  $V_{IL}$  and  $V_{IH}$ . For the purposes of this specification the following conditions apply: a) All input signals are defined as:  $V_{IL} = 0.4V$ ,  $V_{IH} = 2.7V$ ,  $t_R < 10$  ns,  $t_F < 10$  ns. b)  $t_R$  is measured from  $V_{IL}$  to  $V_{IH}$ .  $t_F$  is measured from  $V_{IH}$  to  $V_{IL}$ . c) Delay Times are measured from the input signal Valid to the output signal Valid. d) Setup Times are measured from the data input Valid to the clock input Invalid. e) Hold Times are measured from the clock signal Valid to the data input Invalid. f) Pulse widths are measured from  $V_{IL}$  to  $V_{IL}$  or from  $V_{IH}$  to  $V_{IH}$ .
- (2) See definitions and timing conventions section.

## Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5V \pm 5\%$ ;  $V_{BB} = -5V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ . All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at  $V_{CC} = +5V$ ,  $V_{BB} = -5V$ ,  $T_A = 25^\circ C$ .

All timing parameters are measured at  $V_{OH} = 2.0V$  and  $V_{OL} = 0.7V$ .

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>MASTER CLOCK TIMING</b>						
$f_{MCLK}$	Frequency of MCLK	Selection of Frequency is Programmable (See <a href="#">Table 5</a> )		512		kHz
				1536		kHz
				1544		kHz
				2048		kHz
				<b>4096</b>		kHz
$t_{WMH}$	Period of MCLK High	Measured from $V_{IH}$ to $V_{IH}^{(1)}$	<b>80</b>			ns
$t_{WML}$	Period of MCLK Low	Measured from $V_{IL}$ to $V_{IL}^{(1)}$	<b>80</b>			ns
$t_{RM}$	Rise Time of MCLK	Measured from $V_{IL}$ to $V_{IH}$			30	ns
$t_{FM}$	Fall Time of MCLK	Measured from $V_{IH}$ to $V_{IL}$			30	ns
$t_{HBM}$	HOLD Time, BCLK LOW to MCLK HIGH		<b>50</b>			ns
$t_{WFL}$	Period of $FS_X$ or $FS_R$ Low	Measured from $V_{IL}$ to $V_{IL}$	1			MCLK Period
<b>PCM INTERFACE TIMING</b>						
$f_{BCLK}$	Frequency of BCLK	May Vary from 64 kHz to 4096 kHz in 8 kHz Increments	<b>64</b>		<b>4096</b>	kHz
$t_{WBH}$	Period of BCLK High	Measured from $V_{IH}$ to $V_{IH}$	<b>80</b>			ns
$t_{WBL}$	Period of BCLK Low	Measured from $V_{IL}$ to $V_{IL}$	<b>80</b>			ns
$t_{RB}$	Rise Time of BCLK	Measured from $V_{IL}$ to $V_{IH}$			30	ns
$t_{FB}$	Fall Time of BCLK	Measured from $V_{IH}$ to $V_{IL}$			30	ns
$t_{HBF}$	Hold Time, BCLK Low to $FS_{X/R}$ High or Low		<b>30</b>			ns
$t_{SFB}$	Setup Time, $FS_{X/R}$ High to BCLK Low		<b>30</b>			ns
$t_{DBD}$	Delay Time, BCLK High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads			<b>80</b>	ns
$t_{DBZ}$	Delay Time, BCLK Low to $D_X1$ Disabled if $FS_X$ Low, $FS_X$ Low to $D_X1$ disabled if 8th BCLK Low, or BCLK High to $D_X1$ Disabled if $FS_X$ High	$D_X1$ disabled is measured at $V_{OL}$ or $V_{OH}$ according to <a href="#">Figure 3</a>	<b>15</b>		<b>80</b>	ns
$t_{DBT}$	Delay Time, BCLK High to $\overline{TS}_X$ Low if $FS_X$ High, or $FS_X$ High to $\overline{TS}_X$ Low if BCLK High (Nondelayed mode); BCLK High to $\overline{TS}_X$ Low (delayed data mode)	Load = 100 pF Plus 2 LSTTL Loads			60	ns
$t_{ZBT}$	TRI-STATE Time, BCLK Low to $\overline{TS}_X$ High if $FS_X$ Low, $FS_X$ Low to $\overline{TS}_X$ High if 8th BCLK Low, or BCLK High to $\overline{TS}_X$ High if $FS_X$ High		15		60	ns

(1) Applies only to MCLK Frequencies  $\geq 1.536$  MHz. At 512 kHz a 50:50  $\pm 2\%$  Duty Cycle must be used.

## Timing Specifications (continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5V \pm 5\%$ ;  $V_{BB} = -5V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ . All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at  $V_{CC} = +5V$ ,  $V_{BB} = -5V$ ,  $T_A = 25^\circ C$ .

All timing parameters are measured at  $V_{OH} = 2.0V$  and  $V_{OL} = 0.7V$ .

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{DFD}$	Delay Time, $FS_{X/R}$	Load = 100 pF Plus 2 LSTTL Loads,				
	High to Data Valid	Applies if $FS_{X/R}$ Rises Later Than			<b>80</b>	ns
		BCLK Rising Edge in Non-Delayed Data Mode Only				
$t_{SDB}$	Setup Time, $D_{R1}$		<b>30</b>			ns
	Valid to BCLK Low					
$t_{HBD}$	Hold Time, BCLK		<b>15</b>			ns
	Low to $D_{R1}$ Invalid					
<b>SERIAL CONTROL PORT TIMING</b>						
$f_{CCLK}$	Frequency of CCLK				<b>2048</b>	kHz
$t_{WCH}$	Period of CCLK High	Measured from $V_{IH}$ to $V_{IH}$	<b>160</b>			ns
$t_{WCL}$	Period of CCLK Low	Measured from $V_{IL}$ to $V_{IH}$	<b>160</b>			ns
$t_{RC}$	Rise Time of CCLK	Measured from $V_{IL}$ to $V_{IH}$			50	ns
$t_{FC}$	Fall Time of CCLK	Measured of $V_{IH}$ to $V_{IL}$			50	ns
$t_{HCS}$	Hold Time, CCLK Low	CCLK1	<b>10</b>			ns
	to $\overline{CS}$ Low					
$t_{HSC}$	Hold Time, CCLK	CCLK8	<b>100</b>			ns
	Low to $\overline{CS}$ High					
$t_{SSC}$	Setup Time, $\overline{CS}$		<b>60</b>			ns
	Transition to CCLK Low					
$t_{SSC0}$	Setup Time, $\overline{CS}$	To Insure CO is Not Enabled	60			ns
	Transition to CCLK High	for Single Byte				
$t_{SDC}$	Setup Time, CI		<b>50</b>			ns
	Data In to CCLK Low					
$t_{HCD}$	Hold Time, CCLK		50			ns
	Low to CO Invalid					
$t_{DCD}$	Delay Time, CCLK High	Load = 100 pF Plus 2 LSTTL Loads			<b>80</b>	ns
	to CO Data Out Valid					
$t_{DSD}$	Delay Time, $\overline{CS}$ Low	Applies Only if Separate			<b>80</b>	ns
	to CO Valid	$\overline{CS}$ Used for Byte 2				
$t_{DDZ}$	Delay Time, $\overline{CS}$ or 9th CCLK	Applies to Earlier of $\overline{CS}$	15		80	ns
	High to CO High Impedance	High or 9th CCLK High				
<b>INTERFACE LATCH TIMING</b>						
$t_{SLC}$	Setup Time, IL to	Interface Latch Inputs Only	<b>100</b>			ns
	CCLK 8 of Byte 1					
$t_{HCL}$	Hold Time, IL Valid from		50			ns
	8th CCLK Low (Byte 1)					
$t_{DCL}$	Delay Time CCLK8 of	Interface Latch Outputs Only			200	ns
	Byte 2 to IL	$C_L = 50$ pF				

Timing Diagrams

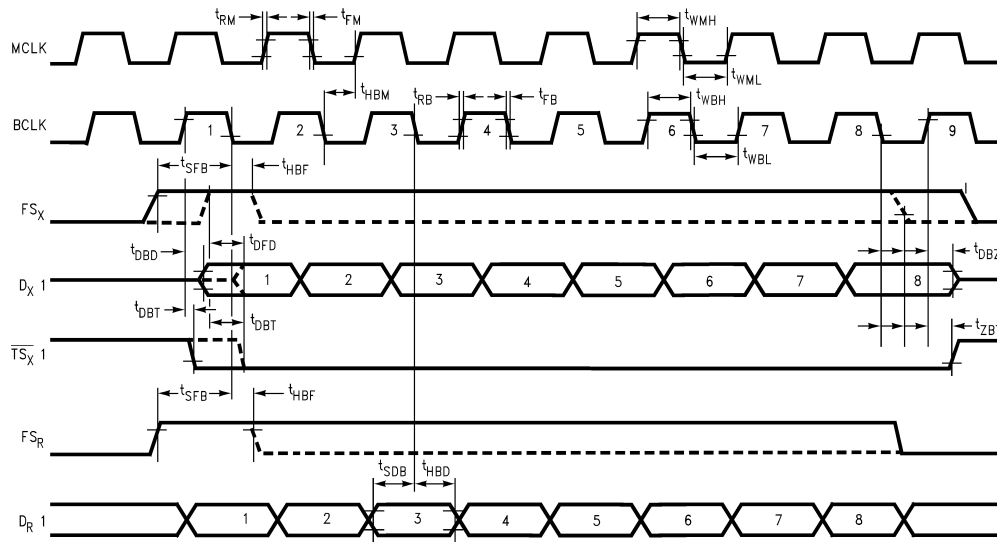


Figure 1. Non-Delayed Data Timing Mode

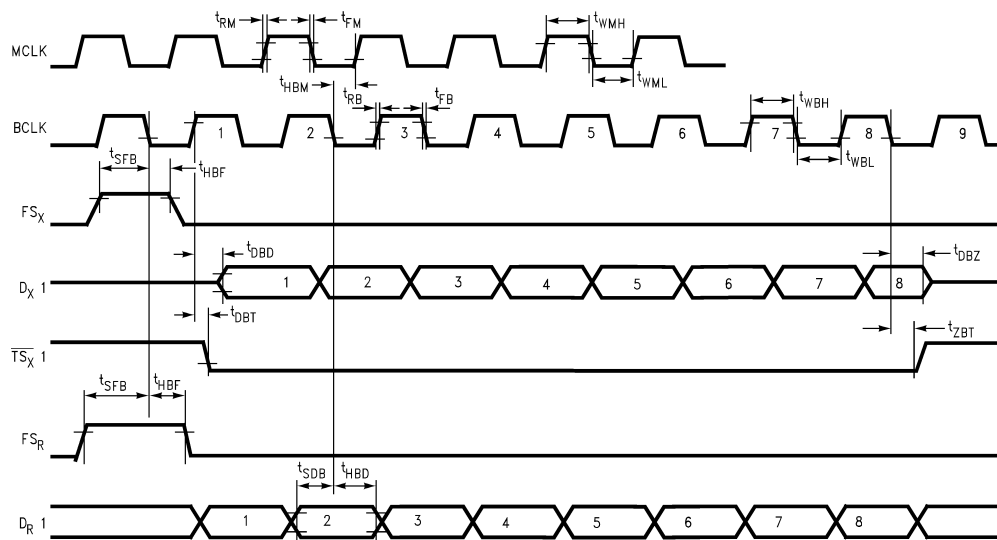


Figure 2. Delayed Data Timing Mode

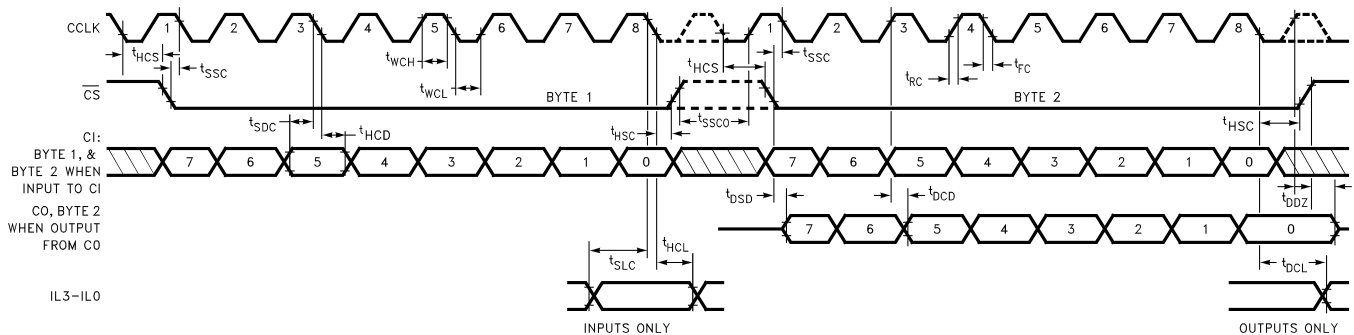


Figure 3. Control Port Timing

## Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ .  $f = 1015.625$  Hz,  $V_{F_XI} = 0$  dBm0,  $D_{R1} = 0$  dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typical values specified at  $V_{CC} = +5V$ ,  $V_{BB} = -5V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>AMPLITUDE RESPONSE</b>						
	Absolute Levels	The Maximum 0 dBm0 Levels Are:				
		$V_{F_XI}$		1.375		Vrms
		$V_{F_{RO}}$ (15 k $\Omega$ Load)		1.964		Vrms
		The Minimum 0 dBm0 Levels are:				
		$V_{F_XI}$		73.8		mVrms
		$V_{F_{RO}}$ (Any Load $\geq 300\Omega$ )		105.0		mVrms
$G_{XA}$	Transmit Gain	Transmit Gain Programmed for Maximum				
	Absolute Accuracy	0 dBm0 Test Level.				
		Measure Deviation of Digital Code from				
		Ideal 0 dBm0 PCM Code at $D_X1$ .				
		$T_A = 25^\circ C$	<b>-0.15</b>		<b>0.15</b>	dB
$G_{XAG}$	Transmit Gain	$T_A = 25^\circ C$ , $V_{CC} = 5V$ , $V_{BB} = 5V$				
	Variation with	Programmed Gain from 0 dB to 19 dB				
	Programmed Gain	(0 dBm0 Levels of 1.619 Vrms to 0.182 Vrms)	<b>-0.1</b>		<b>0.1</b>	dB
		Programmed Gain from 19.1 dB to 25.4 dB				
		(0 dBm0 Levels of 0.180 Vrms to 0.087 Vrms)	<b>-0.3</b>		<b>0.3</b>	dB
		<b>NOTE</b> $\pm 0.1$ dB Min/Max is Available as a Selected Part				
$G_{XAF}$	Transmit Gain	Relative to 1015.625 Hz, <sup>(1)</sup>				
	Variation with	Minimum Gain < $G_X$ < Maximum Gain				
	Frequency	$f = 60$ Hz			-26	dB
		$f = 200$ Hz	-1.8		-0.1	dB
		$f = 300$ Hz to 3000 Hz	-0.15		0.15	dB
		$f = 3400$ Hz	-0.7		0.0	dB
		$f = 400$ Hz			-14	dB
		$f \geq 4600$ Hz. Measure Response			-32	dB
		at Alias Frequency from 0 kHz to 4 kHz				
		$G_X = 0.0$ dB, $V_{F_XI} = 1.375$ Vrms				
		Relative to 1015.625 Hz				
		$f = 62.5$ Hz			<b>-24.9</b>	dB
		$f = 203.125$ Hz	<b>-1.7</b>		<b>-0.1</b>	dB
		$f = 343.75$ Hz	<b>-0.15</b>		<b>0.15</b>	dB
		$f = 515.625$ Hz	<b>-0.15</b>		<b>0.15</b>	dB
		$f = 2140.625$ Hz	<b>-0.15</b>		<b>0.15</b>	dB
		$f = 3156.25$ Hz	<b>-0.15</b>		<b>0.15</b>	dB
		$f = 3406.250$ Hz	<b>-0.74</b>		<b>0.0</b>	dB
		$f = 3984.375$ Hz			<b>-13.5</b>	dB
		Relative to 1062.5 Hz <sup>(1)</sup>				

(1) A multi-tone test technique is used.

**Transmission Characteristics (continued)**

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ .  $f = 1015.625$  Hz,  $VF_{\chi I} = 0$  dBm0,  $D_{R1} = 0$  dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typical values specified at  $V_{CC} = +5V$ ,  $V_{BB} = -5V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
		$f = 5250$ Hz, Measure 2750 Hz			<b>-32</b>	dB
		$f = 11750$ Hz, Measure 3750 Hz			<b>-32</b>	dB
		$f = 49750$ Hz, Measure 1750 Hz			<b>-32</b>	dB
$G_{XAT}$	Transmit Gain	Measured Relative to $G_{XA}$ , $V_{CC} = 5V$ ,				
	Variation with	$V_{BB} = -5V$ ,	-0.1		0.1	dB
	Temperature	Minimum gain < $G_X$ < Maximum Gain				
$G_{XAL}$	Transmit Gain	Sinusoidal Test Method.				
	Variation with	Reference Level = 0 dBm0				
	Signal Level	$VF_{\chi I} = -40$ dBm0 to +3 dBm0	<b>-0.2</b>		<b>0.2</b>	dB
		$VF_{\chi I} = -50$ dBm0 to -40 dBm0	<b>-0.4</b>		<b>0.4</b>	dB
		$VF_{\chi I} = -55$ dBm0 to -50 dBm0	<b>-1.2</b>		<b>1.2</b>	dB
$G_{RA}$	Receive Gain	Receive Gain Programmed for Maximum				
	Absolute Accuracy	0 dBm0 Test Level. Apply 0 dBm0	<b>-0.15</b>		<b>0.15</b>	dB
		PCM Code to $D_{R1}$ . Measure $VF_{R0}$ .				
		$T_A = 25^\circ C$				
$G_{RAG}$	Receive Gain	$T_A = 25^\circ C$ , $V_{CC} = 5V$ , $V_{BB} = -5V$				
	Variation with	Programmed Gain from 0 dB to 19 dB				
	Programmed Gain	(0 dBm0 Levels of 1.964 Vrms to 0.220 Vrms)	<b>-0.1</b>		<b>0.1</b>	dB
		Programmed Gain from 19.1 dB to 25.4 dB				
		(0 dBm0 Levels of 0.218 Vrms to 0.105 Vrms)	<b>-0.3</b>		<b>0.3</b>	dB
		<hr/> <b>NOTE</b> ±0.1 dB Min/Max is Available as a Selected Part				
$G_{RAT}$	Receive Gain	Measured Relative to $G_{RA}$ .				
	Variation with	$V_{CC} = 5V$ , $V_{BB} = -5V$ .	-0.1		0.1	dB
	Temperature	Minimum Gain < $G_R$ < Maximum Gain				
$G_{RAF}$	Receive Gain	Relative to 1015.625 Hz, <sup>(2)</sup>				
	Variation with	$D_{R1} = 0$ dBm0 Code.				
	Frequency	Minimum Gain < $G_R$ < Maximum Gain				
		$f = 200$ Hz	-0.25		0.15	dB
		$f = 300$ Hz to 3000 Hz	-0.15		0.15	dB
		$f = 3400$ Hz	-0.7		0.0	dB
		$f = 4000$ Hz			-14	dB
		$G_R = 0$ dB, $D_{R1} = 0$ dBm0 Code,				
		$G_X = 0$ dB <sup>(2)</sup>				
		$f = 296.875$ Hz	<b>-0.15</b>		<b>0.15</b>	dB
		$f = 1875.00$ Hz	<b>-0.15</b>		<b>0.15</b>	dB
		$f = 2906.25$ Hz	<b>-0.15</b>		<b>0.15</b>	dB
		$f = 2984.375$ Hz	<b>-0.15</b>		<b>0.15</b>	dB
		$f = 3406.250$ Hz	<b>-0.74</b>		<b>0.0</b>	dB

(2) A multi-tone test technique is used.

### Transmission Characteristics (continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ .  $f = 1015.625$  Hz,  $V_{FXL} = 0$  dBm0,  $D_{R1} = 0$  dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typical values specified at  $V_{CC} = +5V$ ,  $V_{BB} = -5V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
		$f = 3984.375$ Hz			<b>-13.5</b>	dB
$G_{RAL}$	Receive Gain	Sinusoidal Test Method.				
	Variation with Signal Level	Reference Level = 0 dBm0.				
		$D_{R1} = -40$ dBm0 to $+3$ dBm0	<b>-0.2</b>		<b>0.2</b>	dB
		$D_{R1} = -50$ dBm0 to $-40$ dBm0	<b>-0.4</b>		<b>0.4</b>	dB
		$D_{R1} = -55$ dBm0 to $-50$ dBm0	<b>-1.2</b>		<b>1.2</b>	dB
		$DR_1 = 3.1$ dBm0 -0.5				
		$R_L = 600\Omega$ , $G_R = -0.5$ dB	-0.2		0.2	dB
		$R_L = 300\Omega$ , $G_R = 1.2$ dB	-0.2		0.2	dB
<b>ENVELOPE DELAY DISTORTION WITH FREQUENCY</b>						
$D_{XA}$	Tx Delay, Absolute	$f = 1600$ Hz			315	$\mu s$
$D_{XR}$	Tx Delay, Relative to DXA	$f = 500$ Hz– $600$ Hz			220	$\mu s$
		$f = 600$ Hz– $800$ Hz			145	$\mu s$
		$f = 800$ Hz– $1000$ Hz			75	$\mu s$
		$f = 1000$ Hz– $1600$ Hz			40	$\mu s$
		$f = 1600$ Hz– $2600$ Hz			75	$\mu s$
		$f = 2600$ Hz– $2800$ Hz			105	$\mu s$
		$f = 2800$ Hz– $3000$ Hz			155	$\mu s$
$D_{RA}$	Rx Delay, Absolute	$f = 1600$ Hz			200	$\mu s$
$D_{RR}$	Rx Delay, Relative to DRA	$f = 500$ Hz– $1000$ Hz	-40			$\mu s$
		$f = 1000$ Hz– $1600$ Hz	-30			$\mu s$
		$f = 1600$ Hz– $2600$ Hz			90	$\mu s$
		$f = 2600$ Hz– $2800$ Hz			125	$\mu s$
		$f = 2800$ Hz– $3000$ Hz			175	$\mu s$
<b>NOISE</b>						
$N_{XC}$	Transmit Noise, C Message	<sup>(3)</sup> 11111111		12	<b>15</b>	dBrnC0
	Weighted, $\mu$ -Law Selected	in Gain Register				
$N_{XP}$	Transmit Noise, P Message	<sup>(3)</sup> 11111111	-74		<b>-67</b>	dBm0p
	Weighted, A-Law Selected	in Gain Register				
$N_{RC}$	Receive Noise, C Message	PCM Code is Alternating Positive		8	<b>11</b>	dBrnC0
	Weighted, $\mu$ -Law Selected					
$N_{RP}$	Receive Noise, P Message	PCM Code Equals Positive Zero		-82	<b>-79</b>	dBm0p
	Weighted, A-Law Selected					
$N_{RS}$	Noise, Single Frequency	$f = 0$ kHz to $100$ kHz, Loop Around			-53	dBm0
		Measurement, $V_{FXL} = 0$ Vrms				
$PPSR_X$	Positive Power Supply	$V_{CC} = 5.0 V_{DC} + 100$ mVrms				
	Rejection, Transmit	$f = 0$ kHz– $4$ kHz <sup>(4)</sup>	<b>36</b>			dBc
		$f = 4$ kHz– $50$ kHz	30			dBc
$NPSR_X$	Negative Power Supply	$V_{BB} = -5.0 V_{DC} + 100$ mVrms				
	Rejection, Transmit	$f = 0$ kHz– $4$ kHz <sup>(4)</sup>	<b>36</b>			dBc
		$f = 4$ kHz– $50$ kHz	30			dBc

(3) Measured by grounded input at  $V_{FXL}$ .(4)  $PPSR_X$ ,  $NPSR_X$ , and  $CT_{R-X}$  are measured with a  $-50$  dBm0 activation signal applied to  $V_{FXL}$ .



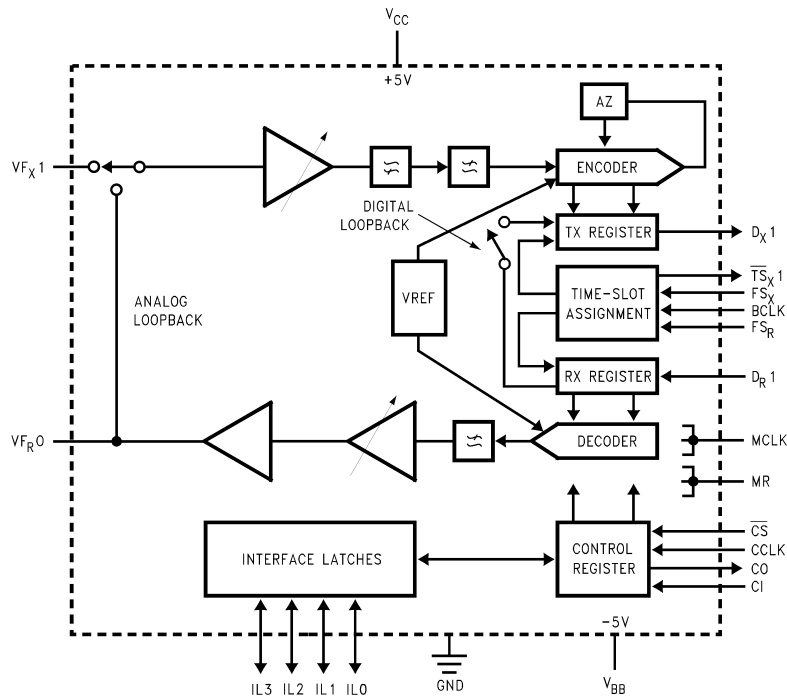
**Transmission Characteristics (continued)**

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{CC} = +5V \pm 5\%$ ,  $V_{BB} = -5V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$  by correlation with 100% electrical testing at  $T_A = 25^\circ C$ .  $f = 1015.625$  Hz,  $VF_{Xl} = 0$  dBm0,  $D_{R1} = 0$  dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typical values specified at  $V_{CC} = +5V$ ,  $V_{BB} = -5V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PPSR <sub>R</sub>	Positive Power Supply	PCM Code Equals Positive Zero				
	Rejection, Receive	$V_{CC} = 5.0 V_{DC} + 100$ mVrms				
		Measure $VF_{RO}$				
		$f = 0$ Hz–4000 Hz	<b>36</b>			dBC
		$f = 4$ kHz–25 kHz	40			dB
		$f = 25$ kHz–50 kHz	36			dB
NPSR <sub>R</sub>	Negative Power Supply	PCM Code Equals Positive Zero				
	Rejection, Receive	$V_{BB} = -5.0 V_{DC} + 100$ mVrms				
		Measure $VF_{RO}$				
		$f = 0$ Hz–4000 Hz	<b>36</b>			dBC
		$f = 4$ kHz–25 kHz	40			dB
		$f = 25$ kHz–50 kHz	36			dB
SOS	Spurious Out-of-Band	0 dBm0 300 Hz to 3400 Hz Input PCM Code				
	Signals Applied at the	at $D_{R1}$				
	Channel Output	4600 Hz–7600 Hz			<b>-30</b>	dB
		7600 Hz–8400 Hz			<b>-40</b>	dB
		8400 Hz–50,000 Hz			<b>-30</b>	dB
<b>DISTORTION</b>						
STD <sub>X</sub>	Signal to Total Distortion	Sinusoidal Test Method				
STD <sub>R</sub>	Transmit or Receive	Level = 3.0 dBm0	<b>33</b>			dBC
	Half-Channel, $\mu$ -Law	= 0 dBm0 to -30 dBm0	<b>36</b>			dBC
	Selected	= -40 dBm0	<b>30</b>			dBC
		= -45 dBm0	<b>25</b>			dBC
STD <sub>RL</sub>	Single to Total Distortion	Sinusoidal Test Method				
	Receive with Resistive	Level = +3.1 dBm0				
	Load	$R_L = 600\Omega$ , $G_R = -0.5$ dB	<b>33</b>			dBC
		$R_L = 300\Omega$ , $G_R = -1.2$ dB	<b>33</b>			dBC
SFD <sub>X</sub>	Single Frequency				<b>-46</b>	dB
	Distortion, Transmit					
SFD <sub>R</sub>	Single Frequency				<b>-46</b>	dB
	Distortion, Receive					
IMD	Intermodulation Distortion	Transmit or Receive				
		Two Frequencies in the Range			<b>-41</b>	dB
		300 Hz–3400 Hz				
<b>CROSSTALK</b>						
CT <sub>X-R</sub>	Transmit to Receive Crosstalk,	$f = 300$ Hz–3400 Hz		-90	<b>-75</b>	dB
	0 dBm0 Transmit Level	$D_R =$ Idle Code				
CT <sub>R-X</sub>	Receive to Transmit Crosstalk,	$f = 300$ Hz–3400 Hz		-90	<b>-70</b>	dB
	0 dBm0 Receive Level	<sup>(5)</sup>				

(5) PPSR<sub>X</sub>, NPSR<sub>X</sub>, and CT<sub>R-X</sub> are measured with a -50 dBm0 activation signal applied to  $VF_{Xl}$ .

Block Diagram



Connection Diagram

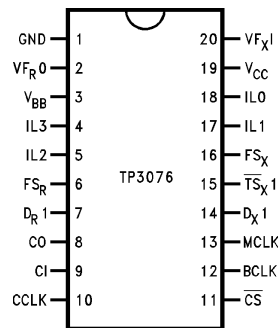


Figure 4.

## PIN FUNCTIONS

### Pin Descriptions

Pin	Description
V <sub>CC</sub>	+5V ±5% power supply.
V <sub>BB</sub>	–5V ±5% power supply.
GND	Ground. All analog and digital signals are referenced to this pin.
FS <sub>X</sub>	Transmit Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the transmit time slot assigned to this device (non-delayed data timing mode), or the start of the transmit frame (delayed data timing mode using the internal time-slot assignment counter).
FS <sub>R</sub>	Receive Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the receive time slot assigned to this device (non-delayed data timing mode), or the start of the receive frame (delayed data timing mode using the internal time-slot assignment counter).
BCLK	Bit clock input used to shift PCM data into and out of the D <sub>R</sub> and D <sub>X</sub> pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1.536/1.544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK.
VF <sub>XI</sub>	The Transmit analog high-impedance input. Voice frequency signals present on this input are encoded as an A-law or μ-law PCM bit stream and shifted out on the selected D <sub>X</sub> pin.
VF <sub>RO</sub>	The Receive analog power amplifier output, capable of driving load impedances as low as 300Ω (depending on the peak overload level required). PCM data received on the assigned D <sub>R</sub> pin is decoded and appears at this output as voice frequency signals.
D <sub>X1</sub>	This transmit data TRI-STATE <sup>®</sup> output remains in the high impedance state except during the assigned transmit time slot on the assigned port, during which the transmit PCM data byte is shifted out on the rising edges of BCLK.
$\overline{\text{TS}}_{X1}$	Normally this open drain output is floating in a high impedance state except when a time-slot is active on the D <sub>X</sub> output, when the $\overline{\text{TS}}_{X1}$ output pulls low to enable a backplane line-driver.
D <sub>R1</sub>	This receive data input is inactive except during the assigned receive time slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.
CCLK	Control Clock input. This clock shifts serial control information into CI or out from CO when the $\overline{\text{CS}}$ input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI	Control Data Input pin. Serial control information is shifted into COMBO II on this pin when $\overline{\text{CS}}$ is low. Byte 1 of control information is always written into COMBO II, while the direction of byte 2 data is determined by bit 2 of byte 1, as defined in <a href="#">Table 1</a>
CO	Control Data Output pin. Serial control or status information is shifted out of COMBO II on this pin when $\overline{\text{CS}}$ is low.
$\overline{\text{CS}}$	Chip Select input. When this pin is low, control information can be written to or read from COMBO II via CI or CO.
IL3–IL0	Each Interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the Interface Latch Register (ILR) whenever control data is written to COMBO II, while $\overline{\text{CS}}$ is low, and the information is shifted out on the CO pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.

## FUNCTIONAL DESCRIPTION

### POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes the COMBO II and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed for no output, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CO pin is in TRI-STATE condition. Other initial states in the Control Register are indicated in Section 2.0.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

### POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing any of the control instructions into the serial control port with the “P” bit set to “1” as indicated in [Table 1](#). It is recommended that the chip be powered down before writing any additional instructions. In the power-down state, all non-essential circuitry is de-activated and the D<sub>X1</sub> output is in the high impedance TRI-STATE condition.

The data stored in the Gain Control registers, the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains active. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control the SLIC.

### TRANSMIT FILTER AND ENCODER

The Transmit section input, V<sub>F<sub>XI</sub></sub>, is a high impedance input. No external components are necessary to set the gain. Following this is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active pre-filter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or  $\mu$ 255 coding laws, which must be selected by a control instruction during initialization (see [Table 1](#) and [Table 2](#)). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is canceled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165  $\mu$ s (due to the Transmit Filter) plus 125  $\mu$ s (due to encoding delay), which totals 290  $\mu$ s. Data is shifted out on D<sub>X1</sub> during the selected time slot on eight rising edges of BCLK.

## DECODER AND RECEIVER FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the  $D_{R1}$  pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or  $\mu 255$  law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral  $\text{Sin } x/x$  correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Power Amplifier capable of driving a 300 $\Omega$  load to  $\pm 3.5\text{V}$ , a 600 $\Omega$  load to  $\pm 3.8\text{V}$  or a 15 k $\Omega$  load to  $\pm 4.0\text{V}$  at peak overload.

**Table 1. Programmable Register Instructions**

Function	Byte 1 <sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>								Byte 2 <sup>(1)</sup>							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Single Byte Power-Up/Down	P	X	X	X	X	X	0	X	None							
Write Control Register	P	0	0	0	0	0	1	X	See <a href="#">Table 2</a>							
Read-Back Control Register	P	0	0	0	0	1	1	X	See <a href="#">Table 2</a>							
Write to Interface Latch Register	P	0	0	0	1	0	1	X	See <a href="#">Table 4</a>							
Read Interface Latch Register	P	0	0	0	1	1	1	X	See <a href="#">Table 4</a>							
Write Latch Direction Register	P	0	0	1	0	0	1	X	See <a href="#">Table 3</a>							
Read Latch Direction Register	P	0	0	1	0	1	1	X	See <a href="#">Table 3</a>							
Write Receive Gain Register	P	0	1	0	0	0	1	X	See <a href="#">Table 8</a>							
Read Receive Gain Register	P	0	1	0	0	1	1	X	See <a href="#">Table 8</a>							
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See <a href="#">Table 7</a>							
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See <a href="#">Table 7</a>							
Write Receive Time-Slot/Port	P	1	0	0	1	0	1	X	See <a href="#">Table 6</a>							
Read-Back Receive Time-Slot/Port	P	1	0	0	1	1	1	X	See <a href="#">Table 6</a>							
Write Transmit Time-Slot/Port	P	1	0	1	0	0	1	X	See <a href="#">Table 6</a>							
Read-Back Transmit Time-Slot/Port	P	1	0	1	0	1	1	X	See <a href="#">Table 6</a>							

- (1) Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI or CO pin. X = don't care.  
(2) "P" is the power-up/down control bit, see Power-up/Down Control section. ("0" = Power Up, "1" = Power Down)  
(3) Other register address codes are invalid and should not be used.

A decode cycle begins immediately after the assigned receive timeslot, and 10  $\mu\text{s}$  later the Decoder DAC output is updated. The total signal delay is 10  $\mu\text{s}$  plus 120  $\mu\text{s}$  (filter delay) plus 62.5  $\mu\text{s}$  ( $\frac{1}{2}$  frame) which gives approximately 190  $\mu\text{s}$ .

## PCM INTERFACE

The  $FS_X$  and  $FS_R$  frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK HIGH to one MCLK period LOW. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see [Table 2](#)). Non-delayed data mode is similar to long-frame timing on the TP3050/60 series of devices (COMBO); time-slots begin nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode, which is similar to shortframe sync timing on COMBO, in which each FS input must be high at least a half-cycle of BCLK earlier than the timeslot. The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing.

When using Time-Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal Time-Slot Assignment counters.

Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles. During each assigned Transmit time-slot, the  $D_X1$  output shifts data out from the PCM register on the rising edges of BCLK.  $\overline{TS}_X1$  also pulls low for the first  $7\frac{1}{2}$  bit times of the time-slot to control the TRI-STATE Enable of a backplane line-driver. Serial PCM data is shifted into the  $D_R1$  input during each assigned Receive time-slot on the falling edges of BCLK.

## SERIAL CONTROL PORT

Control information and data are written into or read-back from COMBO II via the serial control port consisting of the control clock CCLK, the serial data input, CI, and output, CO, and the Chip Select input,  $\overline{CS}$ . All control instructions require 2 bytes, as listed [Table 1](#), with the exception of a single byte power-up/down command. The Byte 1 bits are used as follows: bit 7 specifies power up or power down; bits 6, 5, 4 and 3 specify the register address, bit 2 specifies whether the instruction is read or write; bit 1 specifies a one or two byte instruction; and bit 0 is not used.

To shift control data into COMBO II, CCLK must be pulsed high 8 times while  $\overline{CS}$  is low. Data on the CI input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide  $\overline{CS}$  pulse or may follow the first contiguously, i.e, it is not mandatory for  $\overline{CS}$  to return high between the first and second control bytes. At the end of CCLK8 in the 2nd control byte the data is loaded into the appropriate programmable register.  $\overline{CS}$  may remain low continuously when programming successive registers, if desired. However,  $\overline{CS}$  must be set high when no data transfers are in progress.

To readback Interface Latch data or status information from COMBO II, the first byte of the appropriate instruction is strobed while  $\overline{CS}$  is low, as defined in [Table 1](#).  $\overline{CS}$  must be kept low, or be taken low again for a further 8 CCLK cycles, during which the data is shifted onto the CO pin on the rising edges of CCLK. When  $\overline{CS}$  is high the CO pin is in the high-impedance TRI-STATE, enabling the CI and CO pins of many devices to be multiplexed together.

If  $\overline{CS}$  returns high during either byte 1 or byte 2 before all eight CCLK pulses of that byte occur, both the bit count and byte count are reset and register contents are not affected. This prevents loss of synchronization in the control interface as well as corruption of register data due to processor interrupt or other problem. When  $\overline{CS}$  returns low again, the device will be ready to accept bit 1 of byte 1 of a new instruction.

## PROGRAMMABLE FUNCTIONS

### POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in [Table 1](#) into COMBO II with the “P” bit set to “0” for power-up or “1” for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down by setting the “P” bit as indicated. When the power-up or down control is entered as a single byte instruction, bit one (1) must be reset to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s),  $D_{X1}$  will remain in the high impedance state until the second  $FS_X$  pulse after power-up.

### CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in [Table 1](#). The second byte has the following bit functions:

**Table 2. Control Register Byte 2 Functions**

Bit Number and Name								Function
7	6	5	4	3	2	1	0	
$F_1$	$F_0$	MA	IA	DN	DL	AL	PP	
0	0							MCLK = 512 kHz
0	1							MCLK = 1.536 MHz
								or 1.544 MHz
1	0							MCLK = 2.048 MHz <sup>(1)</sup>
1	1							MCLK = 4.096 MHz
		0	X					Select $\mu$ 255 Law <sup>(1)</sup>
		1	0					A-Law, Including
								Even Bit
								Inversion
		1	1					A-Law, No Even Bit
								Inversion
				0				Delay Data Timing
				1				Non-Delayed
								Data Timing <sup>(1)</sup>
					0	0		Normal Operation <sup>(1)</sup>
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp
								Enabled in PDN
							1	Power Amp
								Disabled in PDN <sup>(1)</sup>

(1) state at power-on initialization.

### Master Clock Frequency Selection

A Master clock must be provided to COMBO II for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits  $F_1$  and  $F_0$  (see [Table 2](#)) must be set during initialization to select the correct internal divider.

### Coding Law Selection

Bits “MA” and “IA” in [Table 2](#) permit the selection of  $\mu$ 255 coding or A-law coding, with or without even bit inversion.

### Analog Loopback

Analog Loopback mode is entered by setting the “AL” and “DL” bits in the Control Register as shown in [Table 2](#). In the analog loopback mode, the Transmit input  $VF_{XI}$  is isolated from the input pin and internally connected to the  $VF_{RO}$  output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The  $VF_{RO}$  pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop.

### Digital Loopback

Digital Loopback mode is entered by setting the “AL” and “DL” bits in the Control Register as shown in [Table 2](#). This mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-slot at  $D_X1$ . PCM decoding continues and analog output appears at  $VF_{R0}$ . The output can be disabled by programming ‘No Output’ in the Receive Gain Register (see [Table 8](#)).

## INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see [Table 1](#) and [Table 3](#). For minimum power dissipation, unconnected latch pins should be programmed as outputs. For the TP3076, bits 2 and 3 should always be programmed as “1” (outputs).

Bits  $L_3$ – $L_0$  must be set by writing the specific instruction to the LDR with the L bits in the second byte set as follows:

**Table 3. Byte 2 Functions of Latch Direction Register<sup>(1)</sup>**

Byte 2 Bit Number							
7	6	5	4	3	2	1	0
$L_0$	$L_1$	$L_2$	$L_3$	1	1	X	X
$L_n$ Bit				IL Direction			
0				Input			
1				Output			

(1) X = Don't Care



## INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Interface Latch Register (ILR) as shown in [Table 1](#) and [Table 4](#). Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR.

It is recommended that during initialization, the state of IL pins to be configured as outputs should be programmed first followed immediately by the Latch Direction Register.

**Table 4. Interface Latch Data Bit Order**

Bit Number							
7	6	5	4	3	2	1	0
D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	X	X

**Table 5. Coding Law Conventions<sup>(1)</sup>**

	$\mu$ 255 Law		True A-Law with Even Bit Inversion		A-Law without Even Bit Inversion	
	MSB	LSB	MSB	LSB	MSB	LSB
	V <sub>IN</sub> = +Full Scale	1	0000000	1	0101010	1
V <sub>IN</sub> = 0V	1	1111111	1	1010101	1	0000000
	1	1111111	0	1010101	0	0000000
V <sub>IN</sub> = -Full Scale	0	0000000	0	0101010	0	1111111

(1) The MSB is always the first PCM bit shifted in or out of COMBO II.

**Table 6. Time-Slot and Port Assignment Instruction**

Bit Number and Name								Function	
7	6	5	4	3	2	1	0		
EN	PS	T <sub>5</sub>	T <sub>4</sub>	T <sub>3</sub>	T <sub>2</sub>	T <sub>1</sub>	T <sub>0</sub>		
	(1)	(2)							
0	1	X	X	X	X	X	X	Disable D <sub>X</sub> 1 Output (Transmit Instruction)	
								Disable D <sub>R</sub> 1 Input (Receive Instruction)	
1	1	Assign One Binary Coded Time-Slot from 0–63							Enable D <sub>X</sub> 1 Output (Transmit Instruction)
		Assign One Binary Coded Time-Slot from 0–63							Enable D <sub>R</sub> 1 Input (Transmit Instruction)

(1) The “PS” bit MUST be set to “1” for both transmit and receive for the TP3076.

(2) T<sub>5</sub> is the MSB of the time-slot assignment bit field. Time-slot bits should be set to “000000” for both transmit and receive when operating in non-delayed data timing mode.

## TIME-SLOT ASSIGNMENT

COMBO II can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs  $FS_X$  and  $FS_R$ . Time-Slot Assignment may only be used with Delay Data timing; see [Figure 2](#).  $FS_X$  and  $FS_R$  may have any phase relationship with each other in BCLK period increments.

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction as shown in [Table 1](#) and [Table 6](#). The last 6 bits of the second byte indicate the selected time-slot from 0–63 using straight binary notation. When writing a time-slot and port assignment register, if the PCM interface is currently active, it is immediately deactivated to prevent possible bus clashes. A new assignment becomes active on the second frame following the end of the Chip-Select for the second control byte. Rewriting of the register contents should not be performed during the talking period of a connection to prevent waveform distortion caused by loss of a sample which will occur with each register write. The “EN” bit allows the PCM input,  $D_{R1}$ , or output,  $D_{X1}$ , as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the  $FS_X$  and  $FS_R$  pulses conform to the delayed data timing format shown in [Figure 2](#).

## PORT SELECTION

On the TP3076, the “PS” bit MUST always be set to 1.

[Table 6](#) shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

## TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in [Table 1](#) and [Table 7](#). This corresponds to a range of 0 dBm0 levels at  $V_{F_XI}$  between 1.375 Vrms and 0.074 Vrms (equivalent to +5.0 dBm to -20.4 dBm in 600Ω).

To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.07299) \quad (1)$$

and convert to the binary equivalent. Some examples are given in [Table 7](#). A complete tabulation is given in Appendix I of AN-614.

It should be noted that the Transmit (idle channel) Noise and Transmit Signal to Total Distortion are both specified with transmit gain set to 0 dB (gain register set to all ones). At high transmit gains there will be some degradation in noise performance for these parameters. See Application Note AN-614 for more information on this subject.

**Table 7. Byte 2 of Transmit Gain Instruction**

Bit Number	0 dBm0 Test Level (Vrms)
<b>7 6 5 4 3 2 1 0</b>	<b>at <math>V_{F_XI}</math></b>
0 0 0 0 0 0 0 0	No Output <sup>(1)</sup>
0 0 0 0 0 0 0 1	0.074
0 0 0 0 0 0 1 0	0.075
—	—
1 1 1 1 1 1 1 0	1.359
1 1 1 1 1 1 1 1	1.375

(1) Analog signal path is cut off, but  $D_X$  remains active and will output codes representing idle noise.

## RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in [Table 1](#) and [Table 8](#). Note the following restrictions on output drive capability:

1. 0 dBm0 levels  $\leq 1.96$  Vrms at  $V_{FRO}$  may be driven into a load of  $\geq 15$  k $\Omega$  to GND; Receive Gain set to 0 dB (gain register set to all ones).
2. 0 dBm0 levels  $\leq 1.85$  Vrms at  $V_{FRO}$  may be driven into a load of  $\geq 600\Omega$  to GND; Receive Gain set to 0.5 dB.
3. 0 dBm0 levels  $\leq 1.71$  Vrms at  $V_{FRO}$  may be driven into a load of  $\geq 300 \Omega$  to GND. Receive Gain set to  $-1.2$  dB.

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.1043) \quad (2)$$

and convert to the binary equivalent. Some examples are given in [Table 8](#). A complete tabulation is given in Appendix I or AN-614.

**Table 8. Byte 2 of Receive Gain Instruction**

Bit Number	0 dBm0 Test Level (Vrms) at $V_{FRO}$
<b>7 6 5 4 3 2 1 0</b>	
0 0 0 0 0 0 0 0	No Output (Low Z to GND)
0 0 0 0 0 0 0 1	0.105
0 0 0 0 0 0 1 0	0.107
—	—
1 1 1 1 1 1 1 0	1.941
1 1 1 1 1 1 1 1	1.964

**APPLICATIONS INFORMATION**

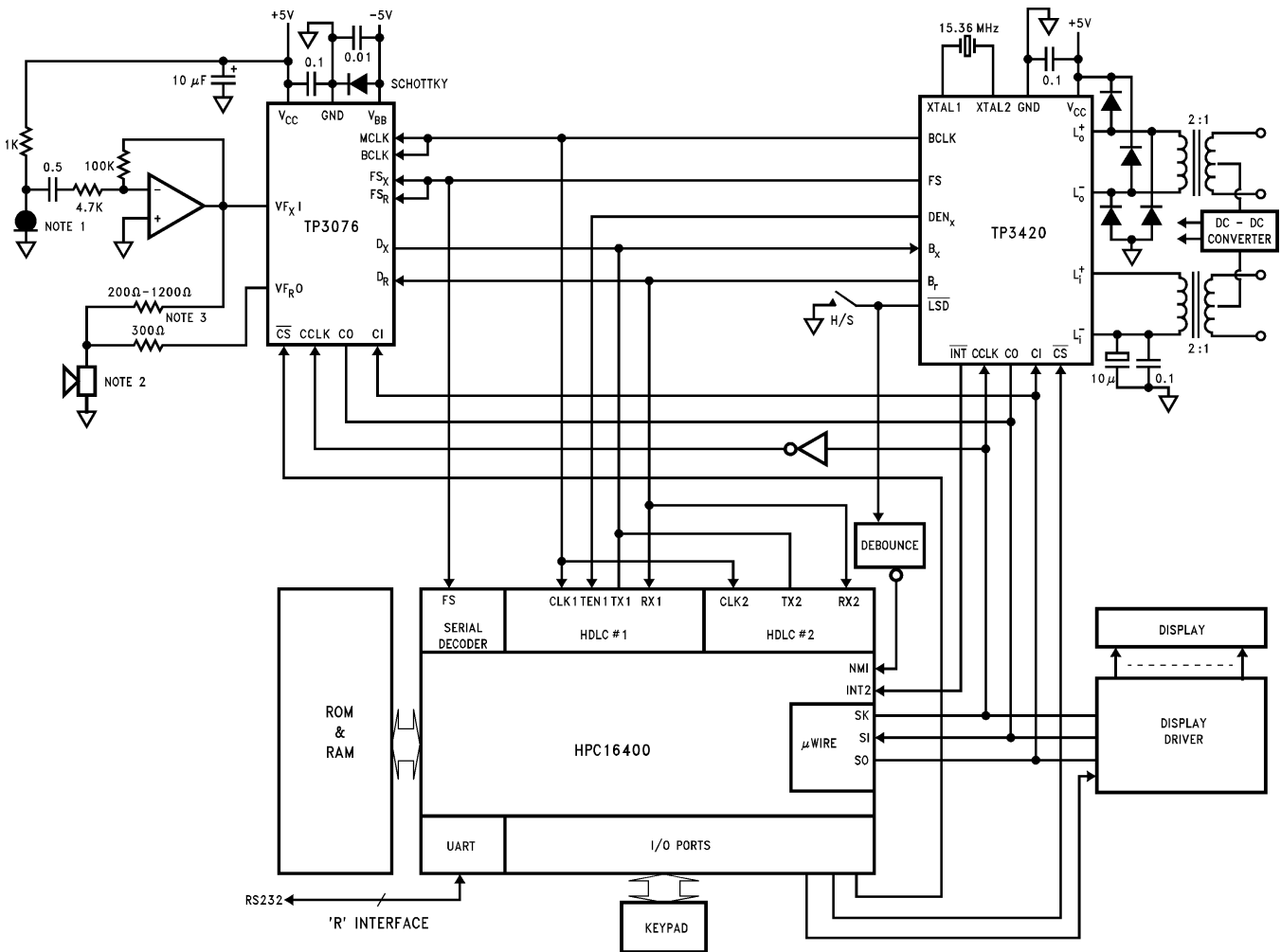
Figure 5 shows a typical ISDN phone application of the TP3076 together with a TP3420 ISDN Transceiver “S” Interface Device and HPC16400 High-Performance Microcontroller with HDLC Controller. The TP3076 device is programmed over its serial control interface via the HPC16400 MICROWIRE/PLUS™ serial I/O port.

**POWER SUPPLIES**

While the pins of the TP3076 COMBO II device are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used and a Schottky diode connected between V<sub>BB</sub> and GND.

To minimize noise sources all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 μF should be connected from this common point to V<sub>CC</sub> and V<sub>BB</sub> as close to the device pins as possible.

Further guidelines on PCB layout techniques are provided in Application Note AN-614, “ COMBO II™ Programmable PCM CODEC/Filter Family Application Guide”.



- (1) Primo type EM80-PMI2 or similar.
- (2) Primo type DH31 or similar.
- (3) Sidetone = -9.2 dB for 200Ω, Sidetone = -21.5 dB for 1200Ω.

**Figure 5. Typical Application in an ISDN Phone**

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