National Semiconductor

PRELIMINARY

microCMOS

TP3401 DASL Digital Adapter for Subscriber Loops

General Description

The TP3401 is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on National's advanced double poly microCMOS process, and requires only a single +5 Volt supply. Alternate Mark Inversion (AMI) line coding, in which binary '1's are alternately transmitted as a positive pulse then a negative pulse, is used to ensure low error rates in the presence of noise with lower emi radiation than other codes such as Bi-phase (Manchester).

Full-duplex transmission at 144 kb/s is achieved on a single twisted wire pair using a burst-mode technique (Time Compression Multiplexed). Thus the device operates as an ISDN 'U' Interface for short loop applications, typically in a PBX environment, providing transmission for 2 B channels and 1 D channel. On #26 cable, the range is at least 1.8 km (6k ft).

System timing is based on a Master/Slave configuration, with the line card end being the Master which controls loop timing and synchronisation. All timing sequences necessary for loop activation and de-activation are generated on-chip. A 2.048 MHz clock, which may be synchronized to the system clock, controls all transmission-related timing functions.

The system is designed to operate on any of the standard types of cable pairs commonly found in premise wiring installations, including mixed gauges from #26AWG to #19AWG. Within certain constraints the system can operate with good margins even when Bridge Taps are present.

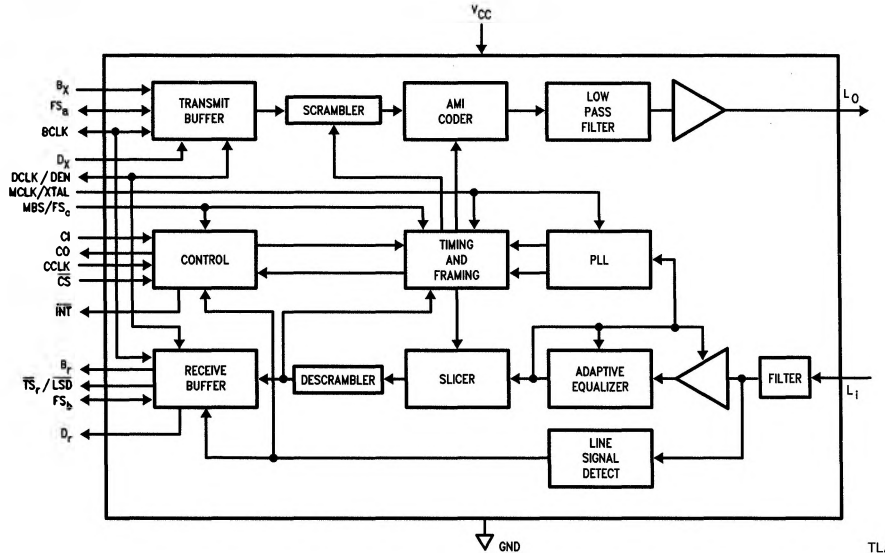
Three serial digital interfaces are provided on the TP3401; one for the transfer of B1 and B2 channel information, one for the transfer of D channel information and a third serial MICROWIRE™ compatible interface for control and status information.

Features

Complete ISDN PBX 2-Wire Data Transceiver including:

- 2 B plus D channel interface for PBX U Interface
- 144 kb/s full-duplex on 1 twisted pair using Burst Mode
- Loop range up to 6 kft (#26AWG)
- Alternate Mark Inversion coding with transmit filter and scrambler for low emi radiation
- Adaptive line equalizer
- On-chip timing recovery, no external components
- System interface with D channel Separate from B
- 2.048 MHz clock
- Driver for line transformer
- 2 loop-back test modes
- +5V only, 80 mW Active Power
- 5 mW idle mode

Block Diagram



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