

60-V, 5- μ A I_Q , 100-mA, Low-Dropout VOLTAGE REGULATOR With Enable and Power-Good

Check for Samples: [TPS7A1601-Q1](#) , [TPS7A1633-Q1](#) , [TPS7A1650-Q1](#)

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C3B
- Wide Input Voltage Range: 3 V to 60 V
- Ultralow Quiescent Current: 5 μA
- Quiescent Current at Shutdown: 1 μA
- Output Current: 100 mA
- Low Dropout Voltage: 60 mV at 20 mA
- Accuracy: 2%
- Available in:
 - Fixed Output Voltage: 3.3 V, 5.0 V
 - Adjustable Version From Approx. 1.2 V to 18.5 V
- Power-Good With Programmable Delay
- Current-Limit and Thermal Shutdown Protections
- Stable With Ceramic Output Capacitors:

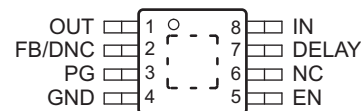
 $\geq 2.2 \mu\text{F}$

- Package: High-Thermal-Performance MSOP-8 PowerPAD™ Package

APPLICATIONS

- High Cell-Count Battery Packs for Power Tools and Other Battery-Powered Microprocessor and Microcontroller Systems
- Car Audio, Navigation, Infotainment, and Other Automotive Systems
- Power Supplies for Notebook PCs, Digital TVs, and Private LAN Systems
- Smoke/ CO_2 Detectors and Battery-Powered Alarm/Security Systems

DGN Package
3-mm \times 5-mm MSOP-8 PowerPAD Package
(Top View)



DESCRIPTION

The TPS7A1633-Q1, TPS7A1601-Q1, and TPS7A1650-Q1 ultralow-power, low-dropout (LDO) voltage regulators offer the benefits of ultralow quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A1633-Q1, TPS7A1601-Q1, and TPS7A1650-Q1 are designed for continuous or sporadic (power backup) battery-powered applications where ultralow quiescent current is critical to extending system battery life.

The TPS7A1633-Q1, TPS7A1601-Q1, and TPS7A1650-Q1 offer an enable pin (EN) compatible with standard CMOS logic and an integrated open-drain active-high power-good output (PG) with a user-programmable delay. These pins are intended for use in microcontroller-based, battery-powered applications where power-rail sequencing is required.

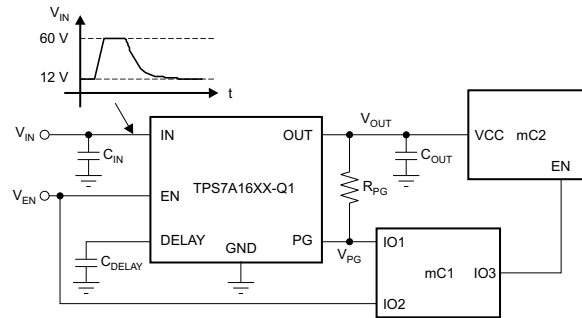
In addition, the TPS7A1633-Q1, TPS7A1601-Q1, and TPS7A1650-Q1 are ideal for generating a low-voltage supply from multicell solutions ranging from high-cell-count power-tool packs to automotive applications; not only can these devices supply a well-regulated voltage rail, but they can also withstand and maintain regulation during voltage transients. These features translate to simpler and more cost-effective, electrical surge-protection circuitry.



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Low-Power Microcontroller Rail Sequencing in Automotive Applications Subject to Load-Dump Transient



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

ORDERABLE PART NUMBER	T _A	PACKAGE		TOP SIDE SYMBOL	STATUS
TPS7A1633QDGNRQ1	–40°C to 125°C	VSSOP - DGN	Reel of 2500	PXYQ	Active
TPS7A1601QDGNRQ1				PXZQ	Active
TPS7A1650QDGNRQ1				PYAQ	Active

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range –40°C ≤ T_J ≤ +125°C (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	IN pin to GND pin	–0.3	62	V
	OUT pin to GND pin	–0.3	20	V
	OUT pin to IN pin	–62	0.3	V
	FB pin to GND pin	–0.3	3	V
	FB pin to IN pin	–62	0.3	V
	EN pin to IN pin	–62	0.3	V
	EN pin to GND pin	–0.3	62	V
	PG pin to GND pin	–0.3	5.5	V
	DELAY pin to GND pin	–0.3	5.5	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T _J , absolute maximum range ⁽²⁾	–40	150	°C
	Storage, T _{stg}	–65	150	°C
Electrostatic discharge rating	Human Body Model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged Device Model (CDM) AEC-Q100 Classification Level C3B		750	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
- (2) Permanent damage does not occur to the part operating within this range, though electrical performance is not guaranteed outside the operating free-air temperature range.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾	TPS7A16xxQDGNRQ1		UNIT
	DGN		
	8 PINS		
θ _{JA} Junction-to-ambient thermal resistance	66.2		°C/W
θ _{JC(top)} Junction-to-case(top) thermal resistance	45.9		°C/W
θ _{JB} Junction-to-board thermal resistance	34.6		°C/W
ψ _{JT} Junction-to-top characterization parameter	1.9		°C/W
ψ _{JB} Junction-to-board characterization parameter	34.3		°C/W
θ _{JC(bottom)} Junction-to-case(bottom) thermal resistance	14.9		°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com).

ELECTRICAL CHARACTERISTICS

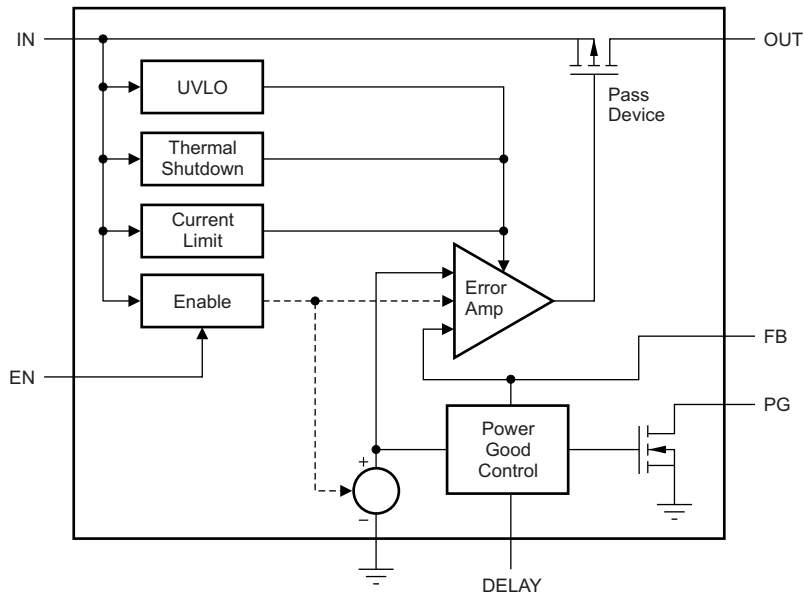
At $T_A = -40^\circ\text{C}$ to 125°C , $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $V_{IN} = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 2.2\ \mu\text{F}$, and FB tied to OUT, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TPS7A16xx-Q1			UNIT
		MIN	TYP	MAX	
V_{IN}	Input voltage range	3		60	V
V_{REF}	Internal reference	1.169	1.193	1.217	V
V_{UVLO}	Undervoltage lockout threshold	2.7			V
V_{OUT}	Output voltage range	$V_{IN} \geq V_{OUT(NOM)} + 0.5\text{ V}$			V
	Nominal accuracy	$T_A = 25^\circ\text{C}$, $V_{IN} = 3\text{ V}$, $I_{OUT} = 10\ \mu\text{A}$			V_{OUT}
	Overall accuracy	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 60\text{ V}^{(1)}$ $10\ \mu\text{A} \leq I_{OUT} \leq 100\text{ mA}$			V_{OUT}
$\Delta V_{O(\Delta VI)}$	Line regulation	$3\text{ V} \leq V_{IN} \leq 60\text{ V}$			V_{OUT}
$\Delta V_{O(\Delta IO)}$	Load regulation	$10\ \mu\text{A} \leq I_{OUT} \leq 100\text{ mA}$			V_{OUT}
V_{DO}	Dropout voltage	$V_{IN} = 4.5\text{ V}$, $V_{OUT(NOM)} = 5\text{ V}$, $I_{OUT} = 20\text{ mA}$			mV
		$V_{IN} = 4.5\text{ V}$, $V_{OUT(NOM)} = 5\text{ V}$, $I_{OUT} = 100\text{ mA}$			265 500
I_{LIM}	Current limit	$V_{OUT} = 90\% V_{OUT(NOM)}$, $V_{IN} = 3.0\text{ V}$			101 225 400
I_{GND}	Ground current	$3\text{ V} \leq V_{IN} \leq 60\text{ V}$, $I_{OUT} = 10\ \mu\text{A}$			5 15
		$I_{OUT} = 100\text{ mA}$			5
I_{SHDN}	Shutdown supply current	$V_{EN} = 0.4\text{ V}$			0.59 5.0
I_{FB}	Feedback current ⁽²⁾				-1 0.0 1
I_{EN}	Enable current	$3\text{ V} \leq V_{IN} \leq 12\text{ V}$, $V_{IN} = V_{EN}$			-1 0.01 1
V_{EN_HI}	Enable high-level voltage				1.2
V_{EN_LO}	Enable low-level voltage				0.3
V_{IT}	PG trip threshold	OUT pin floating, V_{FB} increasing, $V_{IN} \geq V_{IN_MIN}$			85% 95%
		OUT pin floating, V_{FB} decreasing, $V_{IN} \geq V_{IN_MIN}$			83% 93%
V_{HYS}	PG trip hysteresis				2.3% 4%
V_{PG_LO}	PG output low voltage	OUT pin floating, $V_{FB} = 80\% V_{REF}$, $I_{PG} = 1\text{ mA}$			0.4
I_{PG_LKG}	PG leakage current	$V_{PG} = V_{OUT(NOM)}$			-1 1
I_{DELAY}	DELAY pin current				1 2
PSRR	Power-supply rejection ratio	$V_{IN} = 3\text{ V}$, $V_{OUT(NOM)} = V_{REF}$, $C_{OUT} = 10\ \mu\text{F}$, $f = 100\text{ Hz}$			50
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			170
		Reset, temperature decreasing			150
T_A	Operating junction temperature range				-40 125

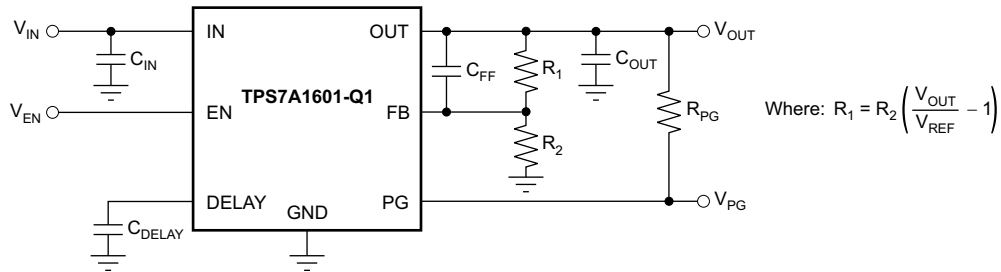
- (1) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P \approx (V_{IN} - V_{OUT}) \times I_{OUT} = (24\text{ V} - V_{REF}) \times 50\text{ mA} \approx 1.14\text{ W}$). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
- (2) $I_{FB} > 0$ flows out of the device.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT

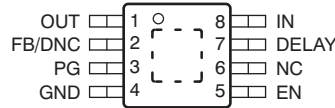


$$\text{Where: } R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

TPS7A1601-Q1 Circuit as an Adjustable Regulator

PIN CONFIGURATION

DGN PACKAGE
 MSOP-8
 (TOP VIEW)



PIN DESCRIPTIONS

TPS7A16xx-Q1		DESCRIPTION
NAME	NO.	
DELAY	7	Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the reset function is not needed.
EN	5	Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN_HI}$, the regulator is enabled. If $V_{EN} \leq V_{EN_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
FB/DNC	2	For the adjustable version (TPS7A1601-Q1), the feedback pin is the input to the control-loop error amplifier. This pin is used to set the output voltage of the device when the regulator output voltage is set by external resistors. For the fixed voltage versions: DO NOT CONNECT to this pin. Do not route this pin to any electrical net, not even GND or IN.
GND	4	Ground pin
IN	8	Regulator input supply pin. A capacitor $> 0.1 \mu\text{F}$ must be tied from this pin to ground to assure stability. It is recommended to connect a $10\text{-}\mu\text{F}$ ceramic capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input tracer or high source impedances are encountered.
NC	6	This pin can be left open or tied to any voltage between GND and IN.
OUT	1	Regulator output pin. A capacitor $> 2.2 \mu\text{F}$ must be tied from this pin to ground to assure stability. It is recommended to connect a $10\text{-}\mu\text{F}$ ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.
PG	3	Power-good pin. Open-collector output; leave open or connect to GND if the power-good function is not needed.
Thermal pad		Solder to printed circuit board (PCB) to enhance thermal performance. Although it can be left floating, it is highly recommended to connect the thermal pad to the GND plane.

TYPICAL CHARACTERISTICS

At $T_A = -40^\circ\text{C}$ to 125°C , $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $V_{IN} = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 2.2\ \mu\text{F}$, and FB tied to OUT, unless otherwise noted.

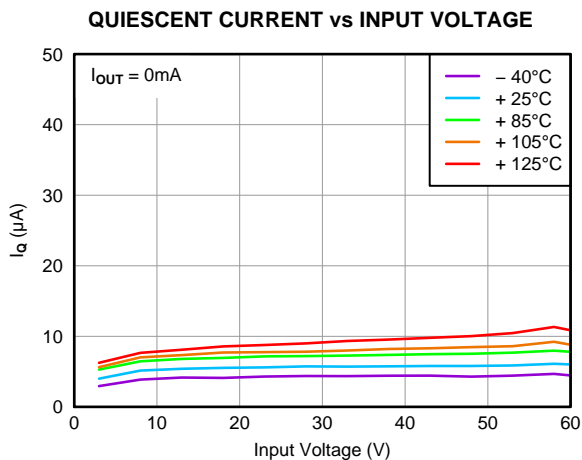


Figure 1.

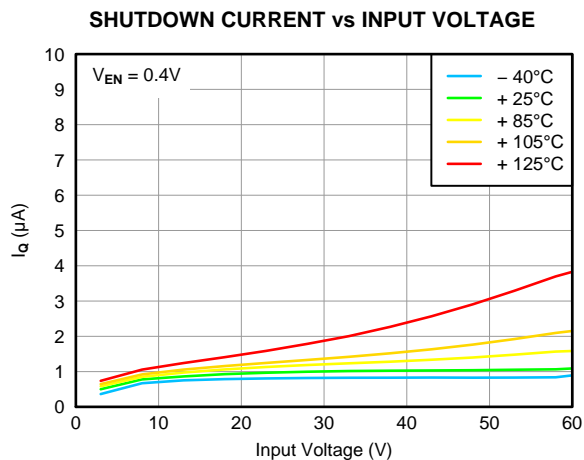


Figure 2.

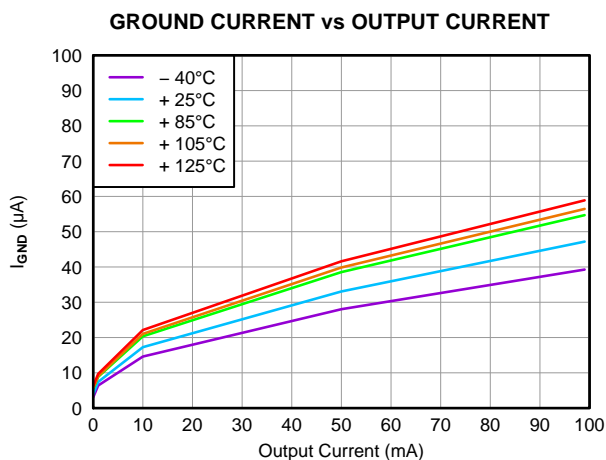


Figure 3.

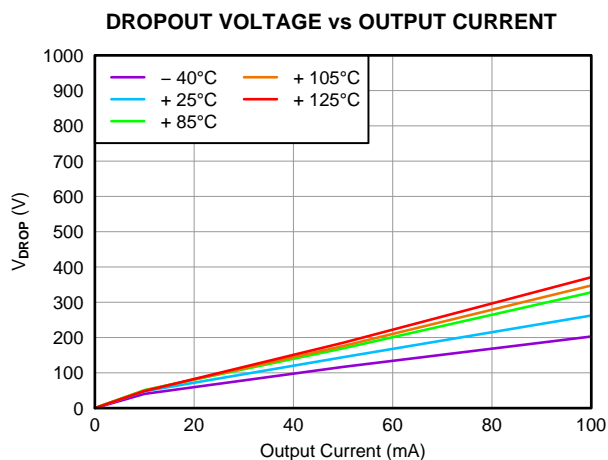


Figure 4.

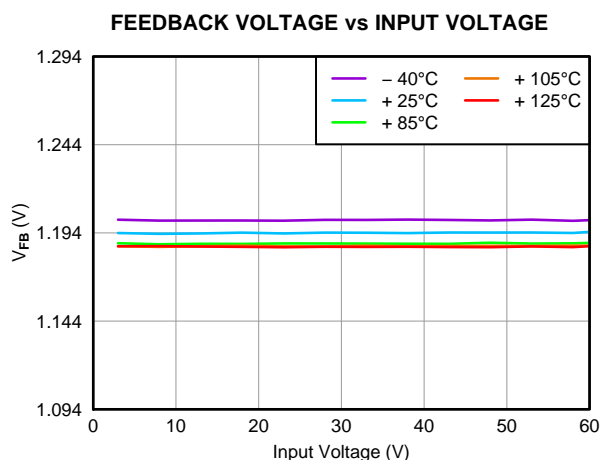


Figure 5.

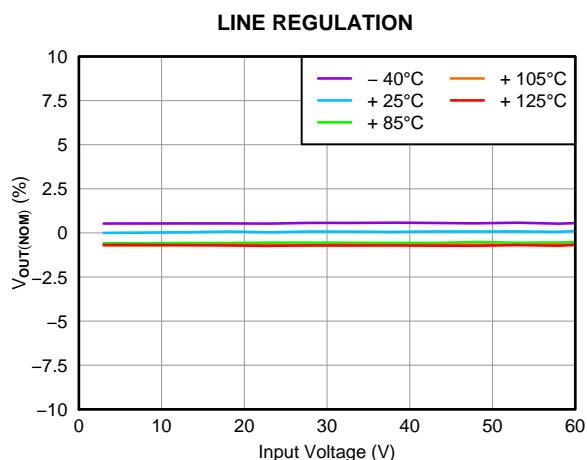


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $V_{IN} = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 2.2\ \mu\text{F}$, and FB tied to OUT, unless otherwise noted.

LOAD REGULATION

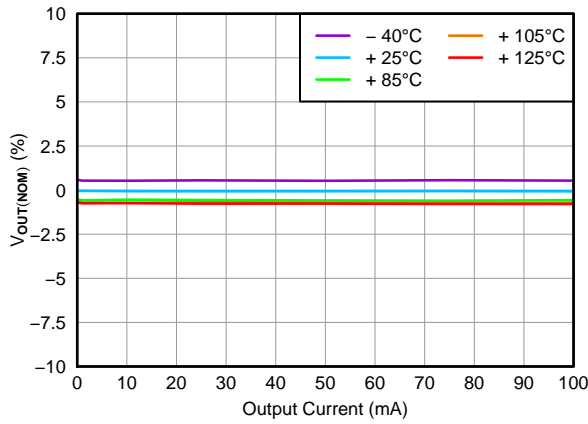


Figure 7.

CURRENT LIMIT vs INPUT VOLTAGE

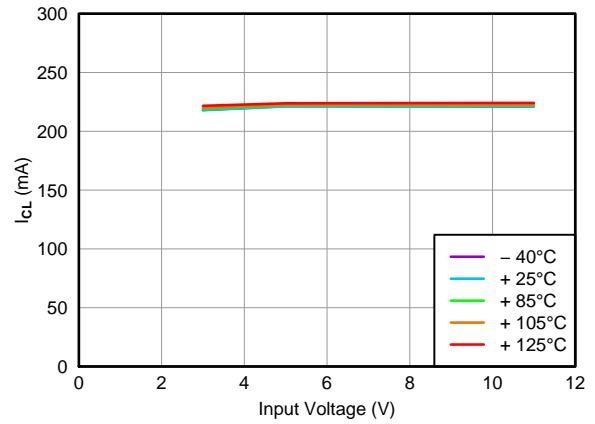


Figure 8.

POWER-GOOD THRESHOLD VOLTAGE vs TEMPERATURE

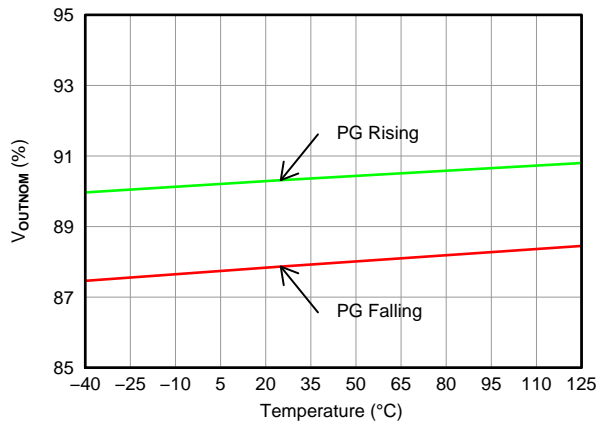


Figure 9.

ENABLE THRESHOLD VOLTAGE vs TEMPERATURE

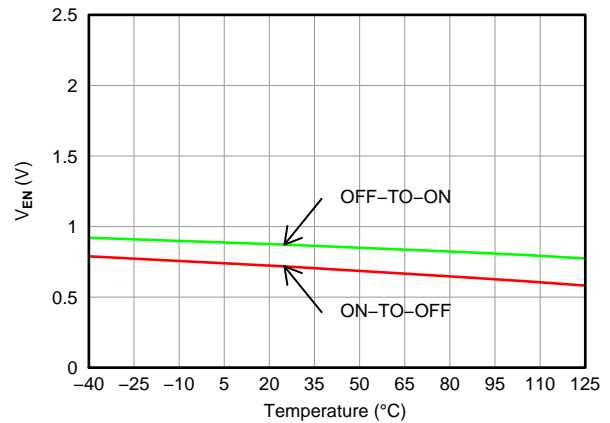


Figure 10.

POWER-SUPPLY REJECTION RATIO

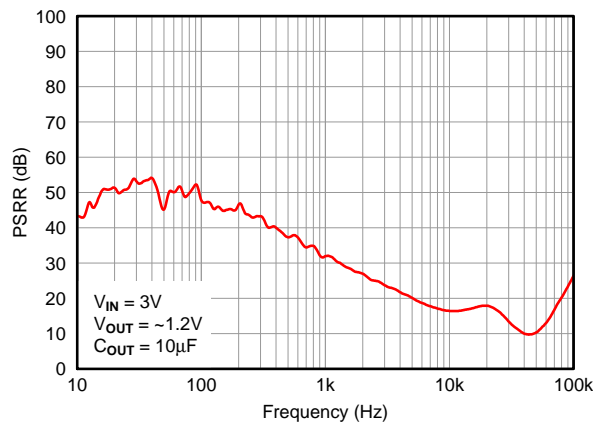


Figure 11.

OUTPUT SPECTRAL NOISE DENSITY

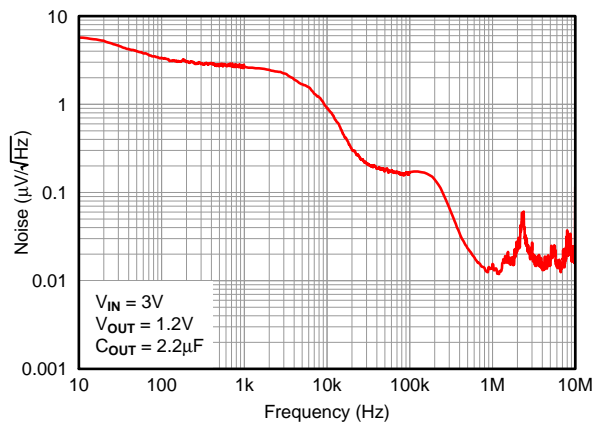


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At $T_A = -40^\circ\text{C}$ to 125°C , $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $V_{IN} = 3\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 10\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 2.2\ \mu\text{F}$, and FB tied to OUT, unless otherwise noted.

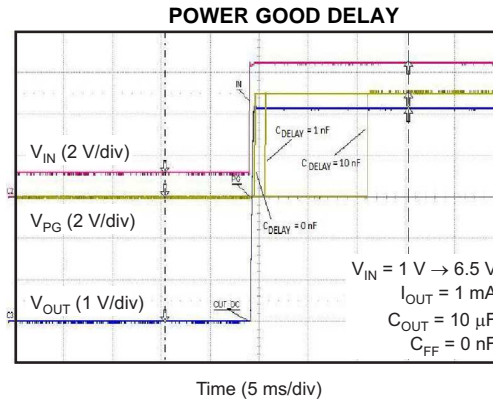


Figure 13.

THEORY OF OPERATION

GENERAL DESCRIPTION

The TPS7A16xx-Q1 family of ultralow-power voltage regulators offers the benefit of ultralow quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16xx-Q1 are designed for continuous or sporadic (power backup) battery-operated applications where ultralow quiescent current is critical to extending system battery life.

ADJUSTABLE VOLTAGE OPERATION

The TPS7A1601-Q1 has an output voltage range from 1.194 V to 20 V. The nominal output of the device is set by two external resistors, as shown in [Figure 14](#):

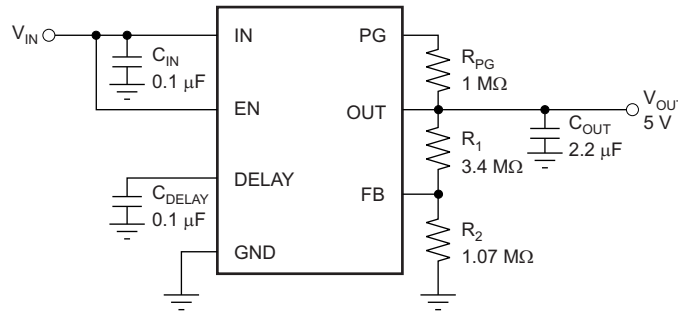


Figure 14. Adjustable Operation

R_1 and R_2 can be calculated for any output voltage range using the formula shown in [Equation 1](#):

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

Resistor Selection

It is recommended to use resistors in the order of $M\Omega$ to keep the overall quiescent current of the system as low as possible (by making the current used by the resistor divider negligible compared to the quiescent current of the device).

If greater voltage accuracy is required, take into account the voltage offset contributions as a result of feedback current and use 0.1% tolerance resistors.

[Table 1](#) shows the resistor combination to achieve an output for a few of the most common rails using commercially available 0.1% tolerance resistors to maximize nominal voltage accuracy, while adhering to the formula shown in [Equation 1](#).

Table 1. Selected Resistor Combinations

V _{OUT}	R ₁	R ₂	V _{OUT} /(R ₁ + R ₂) « I _Q	NOMINAL ACCURACY
1.194 V	0 Ω	∞	0 μA	±2%
1.8 V	1.18 MΩ	2.32 MΩ	514 nA	±(2% + 0.14%)
2.5 V	1.5 MΩ	1.37 MΩ	871 nA	±(2% + 0.16%)
3.3 V	2 MΩ	1.13 MΩ	1056 nA	±(2% + 0.35%)
5 V	3.4 MΩ	1.07 MΩ	1115 nA	±(2% + 0.39%)
10 V	7.87 MΩ	1.07 MΩ	1115 nA	±(2% + 0.42%)
12 V	14.3 MΩ	1.58 MΩ	755 nA	±(2% + 0.18%)
15 V	42.2 MΩ	3.65 MΩ	327 nA	±(2% + 0.19%)
18 V	16.2 MΩ	1.15 MΩ	1038 nA	±(2% + 0.26%)

Close attention must be paid to board contamination when using high-value resistors; board contaminants may significantly impact voltage accuracy. If board cleaning measures cannot be ensured, consider using a fixed-voltage version of the TPS7A16 or using resistors in the order of hundreds or tens of kΩ.

CAPACITOR RECOMMENDATIONS

Low equivalent-series-resistance (ESR) capacitors should be used for the input, output, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high-ESR capacitors may degrade PSRR.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

The TPS7A16xx-Q1 ultralow-power, high-voltage linear regulators achieve stability with a minimum input capacitance of 0.1 μF and output capacitance of 2.2 μF; however, it is recommended to use a 10-μF ceramic capacitor to maximize ac performance.

POWER-GOOD

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. When no C_{DELAY} is used, the PG output is high-impedance when V_{OUT} is greater than the PG trip threshold (V_{IT}). If V_{OUT} drops below V_{IT}, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

To ensure proper operation of the power-good feature, maintain V_{IN} ≥ 3 V (V_{IN_MIN}).

Power-Good Delay and Delay Capacitor

The power-good delay time (t_{DELAY}) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{IT}) to when the PG output is high. This power-good delay time is set by an external capacitor (C_{DELAY}) connected from the DELAY pin to GND; this capacitor is charged from 0 V to up 1.8 V by the DELAY pin current (I_{DELAY}) once V_{OUT} exceeds the PG trip threshold (V_{IT}).

When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT}, and V_{DELAY} exceeds V_{REF}.

The power-good delay time can be calculated using: t_{DELAY} = (C_{DELAY} × V_{REF})/I_{DELAY}. For example, when C_{DELAY} = 10 nF, the PG delay time is approximately 12 ms; that is, (10 nF × 1.193 V)/1 μA = 11.93 ms.

FEED-FORWARD CAPACITOR

Although a feed-forward capacitor (C_{FF}) from OUT to FB is not needed to achieve stability, it is recommended to use a 0.01-μF feed-forward capacitor to maximize ac performance.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases the duration of the transient response.

APPLICATION INFORMATION

AUTOMOTIVE APPLICATIONS

The TPS7A16xx-Q1 maximum input voltage of 60 V makes it ideal for use in automotive applications where high-voltage transients are present.

Events such as load-dump overvoltage (where the battery is disconnected while the alternator is providing current to a load) may cause voltage spikes from 25 V to 60 V. In order to prevent any damage to sensitive circuitry, local transient voltage suppressors can be used to cap voltage spikes to lower, more manageable voltages.

The TPS7A16xx-Q1 can be used to simplify and lower costs in such cases. The very high voltage range allows this regulator not only to withstand the voltages coming out of these local transient voltage suppressors, but even replace them, thus lowering system cost and complexity.

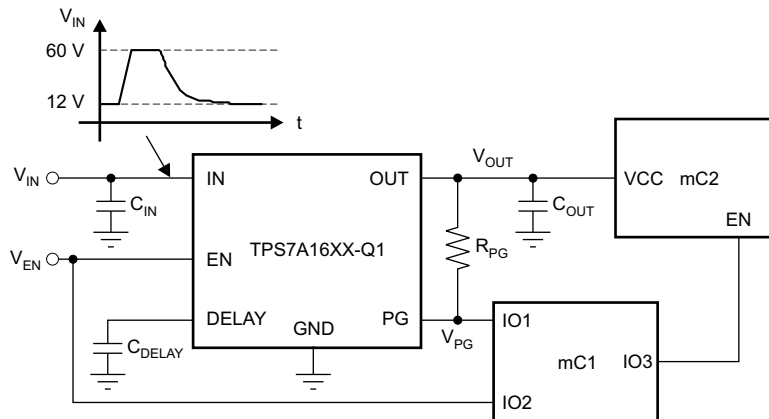


Figure 15. Low-Power Microcontroller Rail Sequencing in Automotive Applications Subjected to Load-Dump Transients

MULTICELL BATTERY PACKS

Currently, battery packs can employ up to a dozen cells in series that, when fully charged, may have voltages of up to 55 V. Internal circuitry in these battery packs is used to prevent overcurrent and overvoltage conditions that may degrade battery life or even pose a safety risk; this internal circuitry is often managed by a low-power microcontroller, such as TI's [MSP430](#).

The microcontroller continuously monitors the battery itself, whether the battery is in use or not. Although this microcontroller could be powered by an intermediate voltage taken from the multicell array, this approach unbalances the battery pack itself, degrading its life or adding cost to implement more complex cell balancing topologies.

The best approach to power this microcontroller is to regulate down the voltage from the entire array to discharge every cell equally and prevent any balancing issues. This approach reduces system complexity and cost.

TPS7A16xx-Q1 is the ideal regulator for this application because it can handle very high voltages (from the entire multicell array) and has very low quiescent current (to maximize battery life).

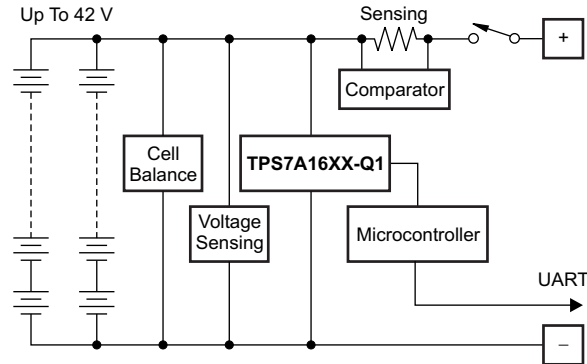


Figure 16. Protection Based on Low-Power Microcontroller Power From Multicell Battery Packs

BATTERY-OPERATED POWER TOOLS

High-voltage multicell battery packs support high-power applications, such as power tools, with high current drain when in use, highly intermittent use cycles, and physical separation between battery and motor.

In these applications, a microcontroller or microprocessor controls the motor. This microcontroller must be powered with a low-voltage rail coming from the high-voltage, multicell battery pack; as mentioned previously, powering this microcontroller or microprocessor from an intermediate voltage from the multicell array causes battery-pack life degradation or added system complexity because of cell balancing issues. In addition, this microcontroller or microprocessor must be protected from the high-voltage transients because of the motor inductance.

The TPS7A16xx-Q1 can be used to power the motor-controlled microcontroller or microprocessor; its low quiescent current maximizes battery shelf life, and its very high-voltage capabilities simplify system complexity by replacing voltage suppression filters, thus lowering system cost.

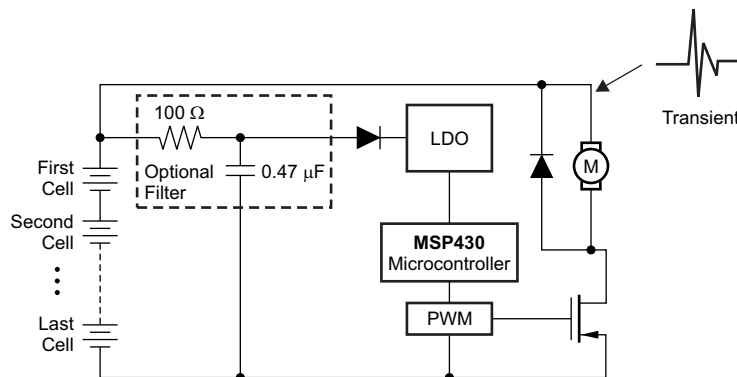


Figure 17. Low Power Microcontroller Power From Multi-Cell Battery Packs In Power Tools

LAYOUT

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS7A16xx-Q1 are available at the end of this product data sheet and at www.ti.com.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7A16xx-Q1 evaluation board, available at www.ti.com.

Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital ICs, such as microcontrollers and microprocessors); these capacitively-coupled signals may produce undesirable output voltage transients. In these cases, it is recommended to use a fixed-voltage version of the TPS7A16xx-Q1, or to isolate the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat-spreading area. For reliable operation, junction temperature should be limited to a maximum of 125°C at the worst case ambient temperature for a given application. To estimate the margin of safety in a complete design (including the copper heat-spreading area), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A16xx-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A16xx-Q1 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

SUGGESTED LAYOUT AND SCHEMATIC

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.

It may be possible to obtain acceptable performance with alternative PCB layouts; however, the layout and the schematic have been shown to produce good results and are meant as a guideline.

Figure 18 shows the schematic for the suggested layout. Figure 19 and Figure 20 show the top and bottom printed circuit board (PCB) layers for the suggested layout.

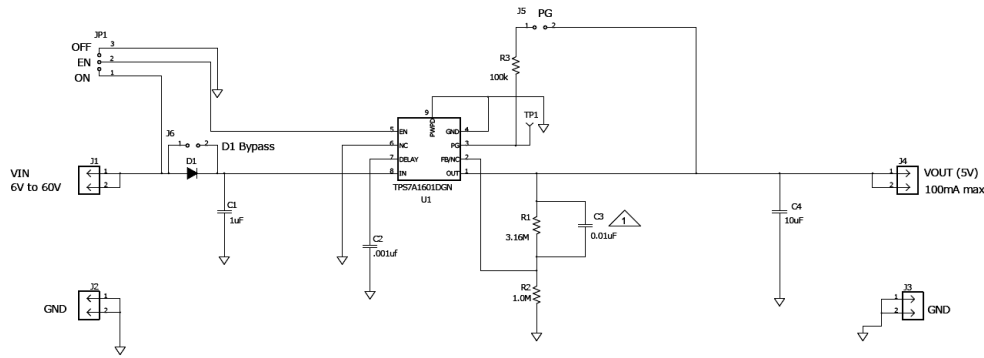


Figure 18. Schematic for Suggested Layout

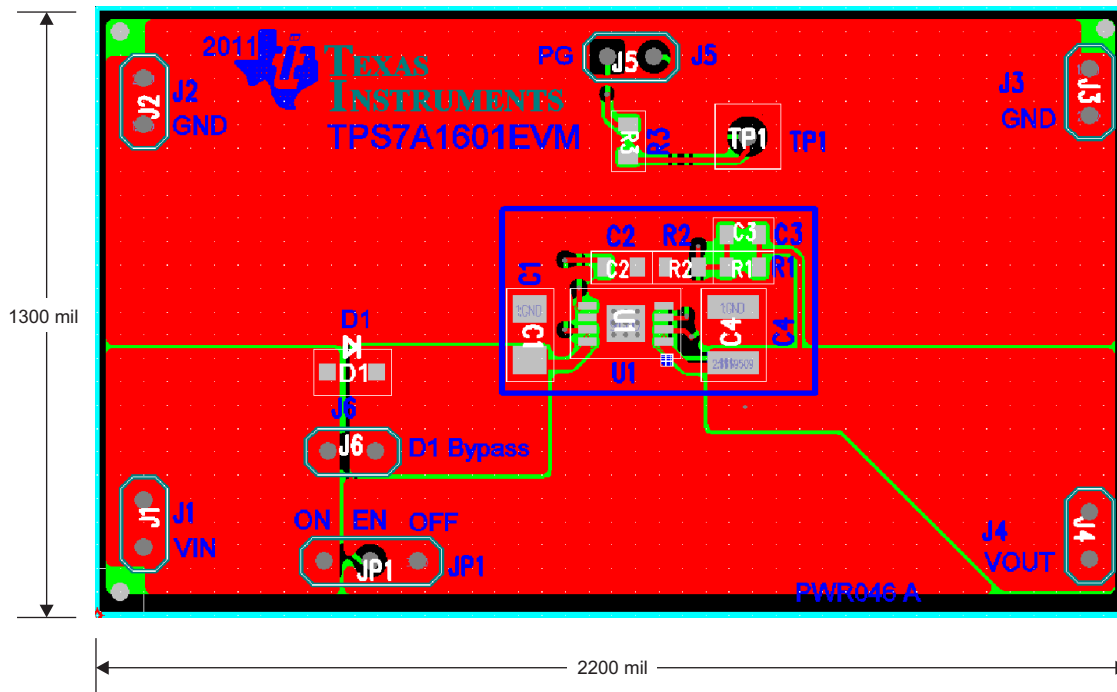


Figure 19. Suggested Layout: Top Layer

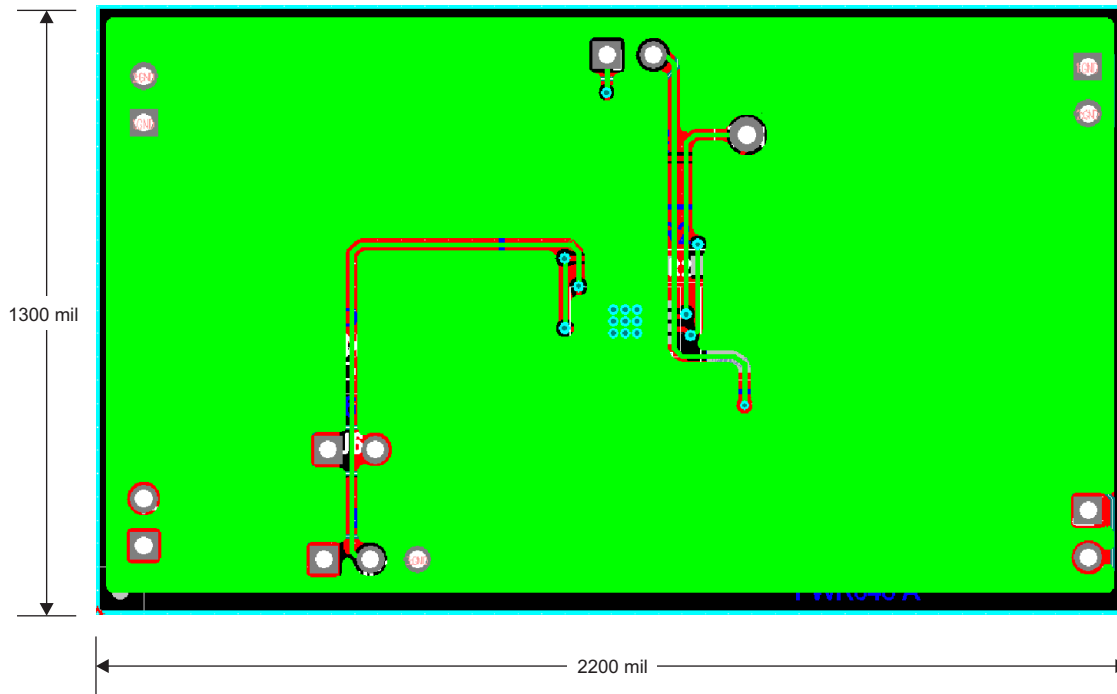





Figure 20. Suggested Layout: Bottom Layer

REVISION HISTORY

Changes from Revision A (March 2012) to Revision B	Page
• Changed to AEC-Q100 Qualified With the Following Results	1
• Changed 2 orderable part numbers from Preview to Active	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS7A1601QDGNRQ1	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		PXZQ	
TPS7A1633QDGNRQ1	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		PXYQ	
TPS7A1650QDGNRQ1	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		PYAQ	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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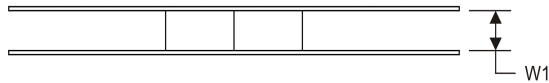
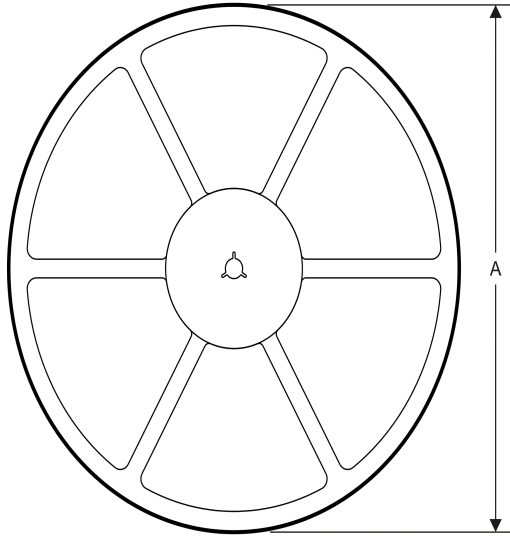
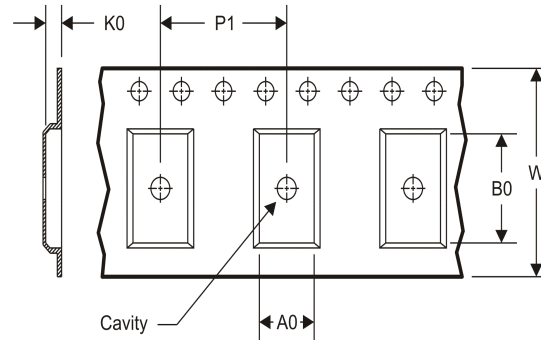
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS7A1601-Q1, TPS7A1633-Q1, TPS7A1650-Q1 :

- Catalog: [TPS7A1601](#), [TPS7A1633](#), [TPS7A1650](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1601QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1633QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1650QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

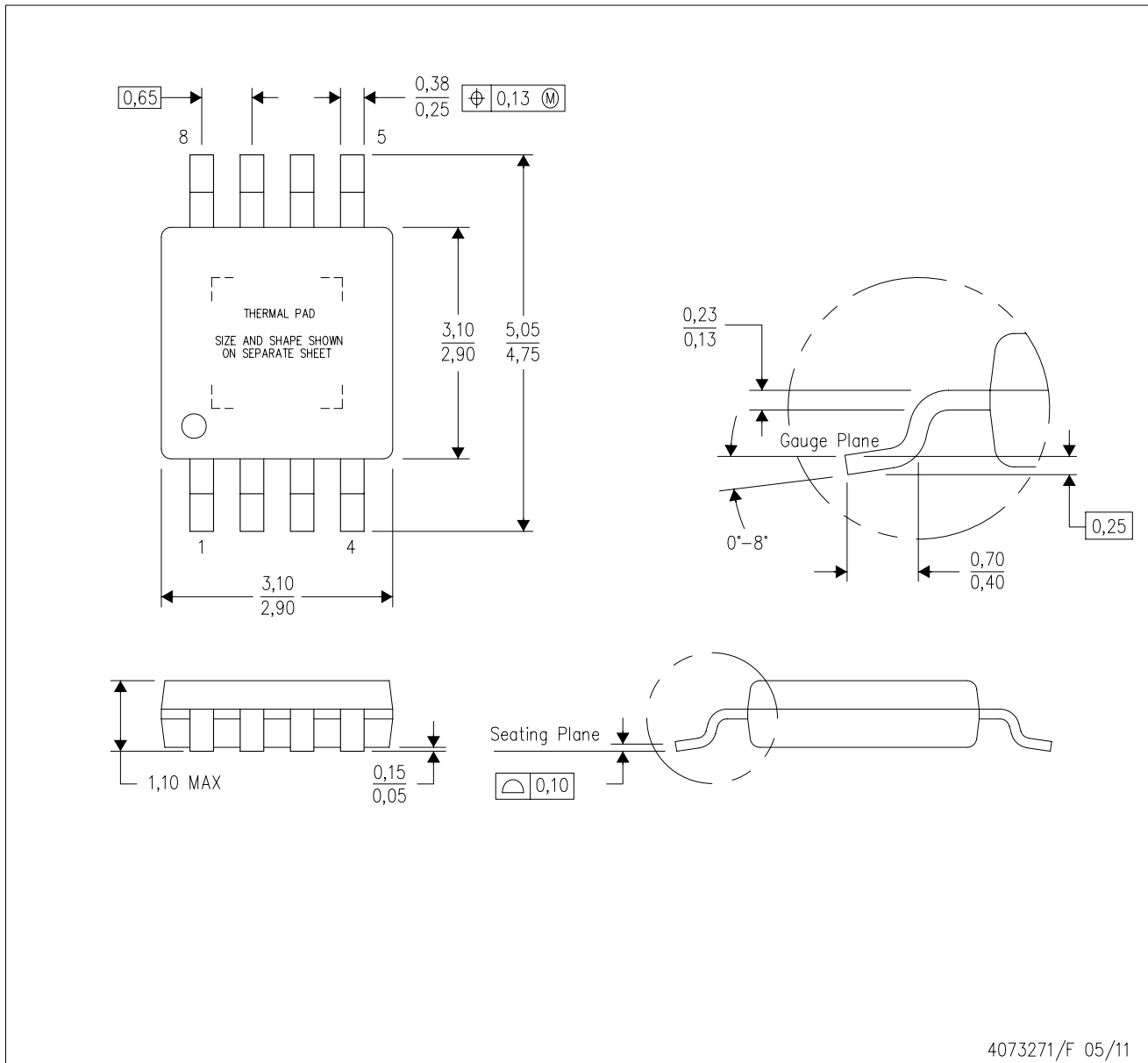
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1601QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS7A1633QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS7A1650QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

DGN (S-PDSO-G8)

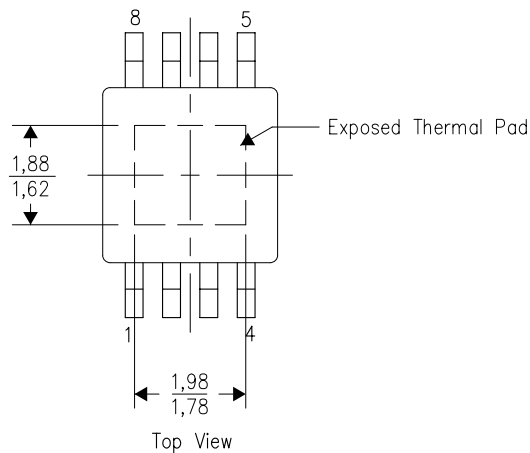
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

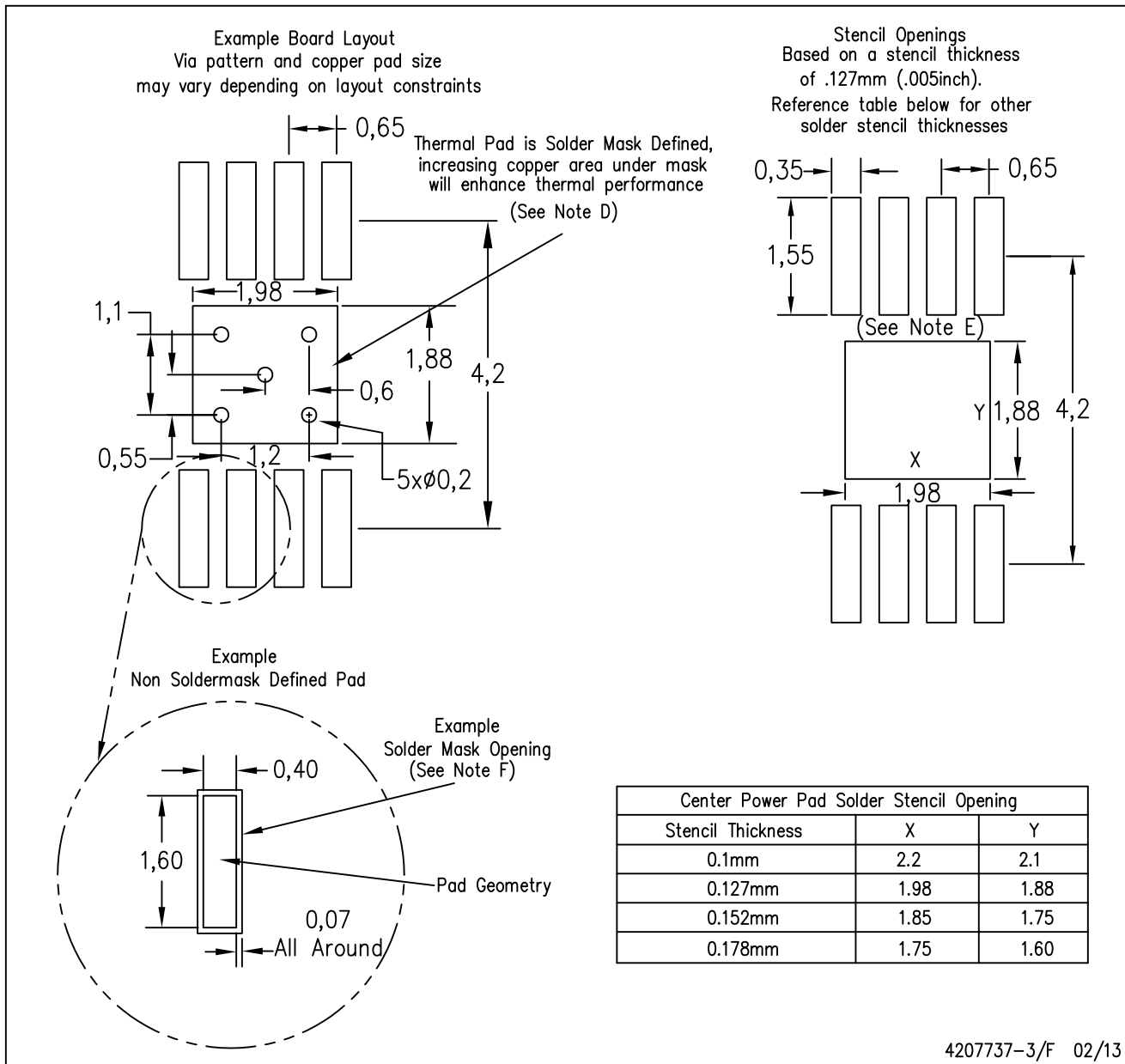


Exposed Thermal Pad Dimensions

4206323-3/1 12/11

NOTE: All linear dimensions are in millimeters

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4207737-3/F 02/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

DGN (S-PDSO-G8)

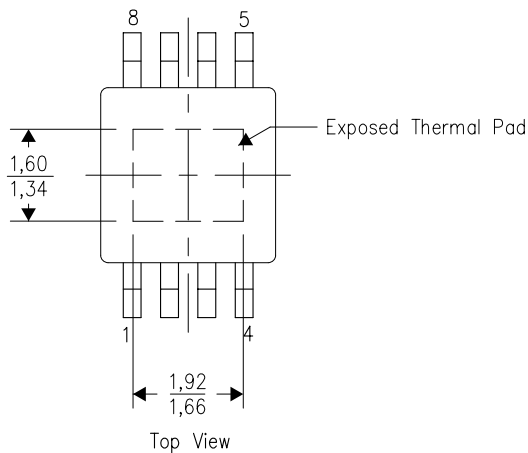
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206323-4/1 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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