

# TUSB1211

## Standalone USB Transceiver Chip

# Data Manual



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Literature Number: SLLSE80A  
March 2011 – Revised January 2012

## Contents

|           |  |                  |
|-----------|--|------------------|
| <b>1</b>  | <b>Features</b> .....                                      | <b><u>5</u></b>  |
| 1.1       | Description .....  | <u>6</u>         |
| <b>2</b>  | <b>Terminal Description</b> .....                          | <b><u>7</u></b>  |
| 2.1       | Terminal Functions .....                                   | <u>7</u>         |
| 2.2       | Block Diagram .....  | <u>9</u>         |
| <b>3</b>  | <b>Electrical Characteristics</b> .....                    | <b><u>10</u></b> |
| 3.1       | Absolute Maximum Ratings .....                             | <u>10</u>        |
| 3.2       | Recommended Operating Conditions .....                     | <u>10</u>        |
| 3.3       | ESD Electrical Parameters .....                            | <u>10</u>        |
| <b>4</b>  | <b>Application Diagram</b> .....                           | <b><u>11</u></b> |
| <b>5</b>  | <b>Clock System</b> .....                                  | <b><u>12</u></b> |
| 5.1       | USB PLL Reference Clock .....                              | <u>12</u>        |
| 5.1.1     | ULPI Input Clock Configuration .....                       | <u>12</u>        |
| 5.1.2     | ULPI Output Clock Configuration .....                      | <u>12</u>        |
| <b>6</b>  | <b>Power Management</b> .....                              | <b><u>14</u></b> |
| 6.1       | Power Provider .....                                       | <u>14</u>        |
| 6.2       | Power Consumption .....                                    | <u>14</u>        |
| 6.3       | Power Control .....  | <u>14</u>        |
| 6.3.1     | Overview .....   | <u>14</u>        |
| <b>7</b>  | <b>USB Transceiver (PHY)</b> .....                         | <b><u>16</u></b> |
| 7.1       | PHY Overview .....   | <u>16</u>        |
| <b>8</b>  | <b>UART Transceiver</b> .....                              | <b><u>17</u></b> |
| <b>9</b>  | <b>USB On-The-Go (OTG) Feature</b> .....                   | <b><u>18</u></b> |
| <b>10</b> | <b>USB Battery Charger Detection and ACA Feature</b> ..... | <b><u>19</u></b> |
| 10.1      | USB Battery Charger Detection Modes .....                  | <u>19</u>        |
| 10.2      | Accessory Charger Adapter (ACA) Detection .....            | <u>19</u>        |

## List of Figures

|     |                                     |                    |
|-----|-------------------------------------|--------------------|
| 2-1 | TFBGA36 Package - Bottom View ..... | <a href="#">7</a>  |
| 4-1 | USB-OTG with ULPI Output Clock..... | <a href="#">11</a> |
| 8-1 | USB UART Data Flow .....            | <a href="#">17</a> |

## List of Tables

|     |  |                    |
|-----|--|--------------------|
| 2-1 | Terminal Functions .....                     | <a href="#">8</a>  |
| 5-1 | Electrical Characteristics: CLOCK Input..... | <a href="#">12</a> |
| 5-2 | Electrical Characteristics: REFCLK .....     | <a href="#">12</a> |
| 6-1 | Summary of Internal Power Providers.....     | <a href="#">14</a> |
| 6-2 | Power Consumption .....                      | <a href="#">14</a> |
| 7-1 | Interface Target Frequencies .....           | <a href="#">16</a> |

# Standalone USB Transceiver Chip

Check for Samples: [TUSB1211](#)

## 1 Features

- **USB2.0 PHY Transceiver Chip, Designed to Interface With a USB Controller via a ULPI Interface, Fully Compliant With:**
  - *Universal Serial Bus Specification Rev. 2.0*
  - *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*
  - *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*
  - *ULPI 12-Pin SDR Interface*
  - *USB Battery Charging Specification Rev. 1.1*
- **USB Battery Charger Detection Feature**
  - Detection Compliant to USB Charging Specification v1.1 Including ACA Detection
  - Additional DP Weak Pullup Resistor Available for Detection of DP/DM Connectivity
- **DP/DM Line External Component Compensation (TI Patent Pending)**
- **Complete USB OTG Physical Front-End that Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)**
- **V<sub>BUS</sub> Overvoltage Protection Circuitry Protects V<sub>BUS</sub> Pin in Range –2 V to 20 V**
- **Internal 5 V Short-Circuit Protection of DP, DM, and ID Pins for Cable Shorting to V<sub>BUS</sub> Pin**
- **ULPI Interface:**
  - I/O Interface (1.8V) Optimized for Non-Terminated 50  $\Omega$  Line Impedance
  - ULPI CLOCK Pin (60 MHz) Supports Both Input and Output Clock Configurations
  - Fully Programmable ULPI-Compliant Register Set
- **Full Industrial Grade Operating Temperature Range from –40°C to 85°C**
- **Available in a TFBGA36 Ball Package**
- **USB HS Start-Of-Frame Clock Output Feature Available on SOF Pin Can be Used to Synchronize Another Application, e.g., Audio, With the USB Packet Stream**
- **Can be Interfaced to Peripheral, Host or OTG Controller Devices via ULPI. Suited to Portable Devices or System ASICs with Built-In Controller Core.**
- **Complete HS-USB Physical Front-End:**
  - Supports High Speed (480 Mbit/s), Full Speed (12 Mbit/s) and Low Speed (1.5 Mbit/s)
  - Integrated Phase-Locked Loop (PLL) Supporting 2 Clock Frequencies 19.2 MHz/26 MHz
  - Integrated 45  $\Omega$   $\pm$ 10% High-Speed Termination Resistors, 1.5 k $\Omega$  Full-Speed Device Pullup Resistor, 15 k $\Omega$  Host Termination Resistors
  - Integrated Transmit and Receive Paths for Parallel-to-Serial and Serial-to-Parallel Data Conversion
  - USB Data Recovery to Allow Recovery of USB Data up to  $\pm$ 500 ppm Frequency Drift
  - Bit-Stuffing Insertion During Transmit and Removal During Receive
  - Non-Return-to-Zero Inverted (NRZI) Encoding and Decoding
  - Supports Bus Reset, Suspend, Resume and High-Speed Detection Handshake (Chirp)
  - HS USB DP/DM Impedance Programmability for External Component Compensation
- **OTG Ver1.3:**
  - Control of External V<sub>BUS</sub> Switch or Charge Pump
  - V<sub>BUS</sub> Fault Detection
  - Both Session Request Protocol (SRP) Methods Supported: Data Pulsing and V<sub>BUS</sub> Pulsing
  - Integrated V<sub>BUS</sub> Detectors and Cable Detection (ID)
- **Internal Power-On Reset (POR) Circuit**
- **Flexible System Integration and Very Low Current Consumption, Optimized for Portable Devices**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## 1.1 Description

The TUSB1211 is a USB2.0 transceiver chip, designed to interface with a USB controller via a ULPI interface. It supports all USB2.0 data rates (High-Speed 480Mbps, Full-Speed 12 Mbps and Low-Speed 1.5Mbps), and is compliant to both Host and Peripheral modes. It additionally supports a UART mode and legacy ULPI serial modes.

TUSB1211 also supports USB Battery Charging Specification Ver1.1. integrating a charger detection module for sensing and control on DP/DM lines, and ACA (Accessory Charger Adapter) detection and control on ID line. ACA allows simultaneous connection of a USB Charger or Charging Downstream Port and an Accessory to a portable OTG device. Configuration bits allow an ACA-agnostic legacy link to correctly communicate with the connected accessory Port through the ACA.

TUSB1211 also supports the OTG (Ver1.3) optional addendum to the USB2.0 specification, including Host Negotiation Protocol (HNP) and Session Request Protocol (SRP).

TUSB1211 is optimized to be interfaced through a 12-pin SDR UTMI Low Pin Interface (ULPI), supporting both input clock and output clock modes, with 1.8 V interface supply voltage.

TUSB1211 integrates a 3.3 V LDO, which makes it flexible to work with either battery operated systems or pure 3.3 V supplied systems. Both the main supply and the 3.3 V power domain can be supplied through an external switched-mode converter for optimized power efficiency.

TUSB1211 includes a POR circuit to detect supply presence on  $V_{BAT}$  and  $V_{DDIO}$  pins. TUSB1211 can be disabled or configured in low power mode for energy saving.

TUSB1211 is protected against accidental shorts to 5 V or ground on its exposed interface (DP/DM/ID). It is also protected against up to 20 V surges on  $V_{BUS}$ .

TUSB1211 integrates a high-performance low-jitter 480 MHz PLL and supports two clock configurations. Depending on the required link configuration, TUSB1211 supports both ULPI input and output clock mode : input clock mode, in which case a square-wave 60 MHz clock is provided to TUSB1211 at the ULPI interface CLOCK pin; and output clock mode in which case TUSB1211 can accept a square-wave reference clock at REFCLK of either 19.2 MHz, 26 MHz. Frequency is indicated to TUSB1211 via the configuration pin CFG. This can be useful if a reference clock is already available in the system.

## 2 Terminal Description

**TFBGA36 PACKAGE  
(BOTTOM VIEW)**

|   |               |                   |        |         |        |        |
|---|---------------|-------------------|--------|---------|--------|--------|
| F | CHRG_<br>POL  | CHRG_<br>DET      | VBAT   | VBUS    | REFCLK | SOF    |
| E | CHRG_<br>EN_N | FAULT             | REG3V3 | GND     | DIR    | REG1V5 |
| D | DP            | GND               | ID     | PSW     | NXT    | STP    |
| C | DM            | NC <sup>(1)</sup> | CS_N   | RESET_N | GND    | DATA7  |
| B | DATA0         | VDDIO             | CS     | CFG     | VDDIO  | DATA6  |
| A | DATA1         | DATA2             | DATA3  | CLOCK   | DATA4  | DATA5  |
|   | 1             | 2                 | 3      | 4       | 5      | 6      |

(1) NC = Not Connected

(2) The size of the device should be 3.5 mm ±0.1 mm by 3.5 mm ±0.1 mm. Height is 1.0 mm typical 1.15 mm max including the solder balls. The pitch of the device is 0.5 mm. Ball width 0.3 mm ±0.05 mm.

**Figure 2-1. TFBGA36 Package - Bottom View**

### 2.1 Terminal Functions

Table 2-1 provides a description of the signals on the TUSB1211 package; some signals are available on multiple pins.

**Table 2-1. Terminal Functions**

| #  | PIN <sup>(1)</sup> | NAME      | A/D <sup>(2)</sup> | TYPE <sup>(3)</sup> | LEVEL <sup>(4)</sup> | DESCRIPTION  |
|----|--------------------|-----------|--------------------|---------------------|----------------------|--|
| 1  | D5                 | NXT       | D                  | O                   | V <sub>DDIO</sub>    | ULPI NXT output signal   |
| 2  | B1                 | DATA0     | D                  | I/O                 | V <sub>DDIO</sub>    | ULPI DATA input/output signal synchronized to CLOCK  |
| 3  | A1                 | DATA1     | D                  | I/O                 | V <sub>DDIO</sub>    | ULPI DATA input/output signal synchronized to CLOCK  |
| 4  | A2                 | DATA2     | D                  | I/O                 | V <sub>DDIO</sub>    | ULPI DATA input/output signal synchronized to CLOCK  |
| 5  | A3                 | DATA3     | D                  | I/O                 | V <sub>DDIO</sub>    | ULPI DATA input/output signal synchronized to CLOCK  |
| 6  | A5                 | DATA4     | D                  | I/O                 | V <sub>DDIO</sub>    | ULPI DATA input/output signal synchronized to CLOCK  |
| 7  | A6                 | DATA5     | D                  | I/O                 | V <sub>DDIO</sub>    | ULPI DATA input/output signal synchronized to CLOCK  |
| 8  | B6                 | DATA6     | D                  | I/O                 | V <sub>DDIO</sub>    | ULPI DATA input/output signal synchronized to CLOCK  |
| 9  | B3                 | CS        | D                  | I                   | VDDIO                | Active-high chip select pin. When low the IC is in power down and ULPI bus is tri-stated. When high (and CS_N pin is tie to VDDIO if unused) normal operation.   |
| 10 | E6                 | REG1V5    | A                  | POWER               | V <sub>DD15</sub>    | 1.5 V internal LDO output. Connect to external filtering capacitor.  |
| 11 | C6                 | DATA7     | D                  | I/O                 | V <sub>DDIO</sub>    | ULPI DATA input/output signal synchronized to CLOCK  |
| 12 | B4                 | CFG       | D                  | I                   | V <sub>DDIO</sub>    | REFCLK clock frequency configuration pin. Two frequencies are supported: 19.2MHz when 0, or 26MHz when 1.  |
| 13 | D1                 | DP        | A                  | I/O                 | V <sub>DD33</sub>    | DP pin of the USB connector  |
| 14 | C1                 | DM        | A                  | I/O                 | V <sub>DD33</sub>    | DM pin of the USB connector  |
| 15 | E3                 | REG3V3    | A                  | POWER               | V <sub>DD33</sub>    | 3.3 V internal LDO output. Connect to external filtering capacitor.  |
| 16 | F3                 | VBAT      | A                  | POWER               | V <sub>BAT</sub>     | Input supply voltage or battery source. Nominally 3.3 V to 4.5 V   |
| 17 | F4                 | VBUS      | A                  | I/O                 | V <sub>BUS</sub>     | VBUS pin of the USB connector  |
| 18 | D3                 | ID        | A                  | I/O                 | V <sub>BUS</sub>     | Identification (ID) pin of the USB connector   |
| 19 | A4                 | CLOCK     | D                  | I/O                 | V <sub>DDIO</sub>    | ULPI 60MHz clock on which ULPI data is synchronized. 2 modes are possible:<br>Input Mode: CLOCK defaults as an input (this is the default clock mode)<br>Output Mode: When an input clock is detected on REFCLK pin then CLOCK will change to an output  |
| 20 | C4                 | RESET_N   | D                  | I                   | V <sub>DDIO</sub>    | Active low chip reset pin. Minimum pulse width 100 $\mu$ s. When low all digital logic (except 32kHz logic required for power-up sequencing and charger detection state-machine) including registers are reset to their default values. ULPI bus is in "ULPI Synchronous mode power-up PLL OFF" state as described in Table14-1. When high normal USB operation.                     |
| 21 | D6                 | STP       | D                  | I                   | V <sub>DDIO</sub>    | ULPI STP input signal  |
| 22 | E5                 | DIR       | D                  | O                   | V <sub>DDIO</sub>    | ULPI DIR output signal   |
| 23 | B5                 | VDDIO     | A                  | I                   | V <sub>DDIO</sub>    | External 1.8V supply input for digital I/Os. Connect to external filtering capacitor.  |
| 24 | B2                 | VDDIO     | A                  | I                   | V <sub>DDIO</sub>    | External 1.8V supply input for digital I/Os. Connect to external filtering capacitor.  |
| 25 | C5                 | GND       | A                  | GROUND              | GND                  | Ground   |
| 26 | D2                 | GND       | A                  | GROUND              | GND                  | Ground   |
| 27 | E4                 | GND       | A                  | GROUND              | GND                  | Ground   |
| 28 | F5                 | REFCLK    | A                  | I                   | V <sub>DDIO</sub>    | Reference clock input.<br>Input reference clock frequency must be indicated by CFG pin.<br>Two frequencies are supported: 19.2MHz (when CFG = 0), and 26MHz (when CFG = 1).  |
| 29 | F6                 | SOF       | D                  | O                   | V <sub>DDIO</sub>    | HS USB SOF (Start-Of-Frame) output clock. (feature controlled by SOF_EN bit, disabled and output logic low by default). HS USB SOF packet rate is 8 kHz  |
| 30 | C2                 | NC        |                    |                     |                      | Not connected  |
| 31 | C3                 | CS_N      | D                  | I                   | V <sub>DDIO</sub>    | Active-low chip select pin. When high the IC is in power down and ULPI bus is tri-stated. When low (and CS pin is high) normal operation. Tie to GND if unused.  |
| 32 | E1                 | CHRG_EN_N | D                  | I                   | V <sub>BAT</sub>     | Active low input pin used to enable Battery Charging Detection in Dead Battery Charger Detection mode. This pin is ignored in ACTIVE mode. Connect to GND to activate. Connect to VBAT when charger detection not required   |
| 33 | E2                 | FAULT     | D                  | I                   | V <sub>BAT</sub>     | VBUS fault detector input used as EXTERNALVBUSINDICATOR in TUSB1211. The link must enable VBUS fault detection via the USEEXTERNALVBUSINDICATOR register bit, and the polarity must be set via the INDICATORCOMPLEMENT register bit. INDICATORPASSTHRU bit can be used to qualify FAULT with the internal vbusvalid comparator. Connect to GND if not used. This pin is 5V tolerant. |
| 34 | F1                 | CHRG_POL  | D                  | I                   | V <sub>BAT</sub>     | When connected to GND then CHRG_DET output pin is active low. When connected to VBAT then CHRG_DET output pin is active high.  |

(1) Pin = Package Pin coordinate of [Figure 2-1](#)

(2) A/D: A = Analog pin, D = Digital pin

(3) TYPE: I = Input pin type, O = Output pin type, I/O = Input/Output pin type, POWER = Power supply pin type, GROUND = Ground type pin

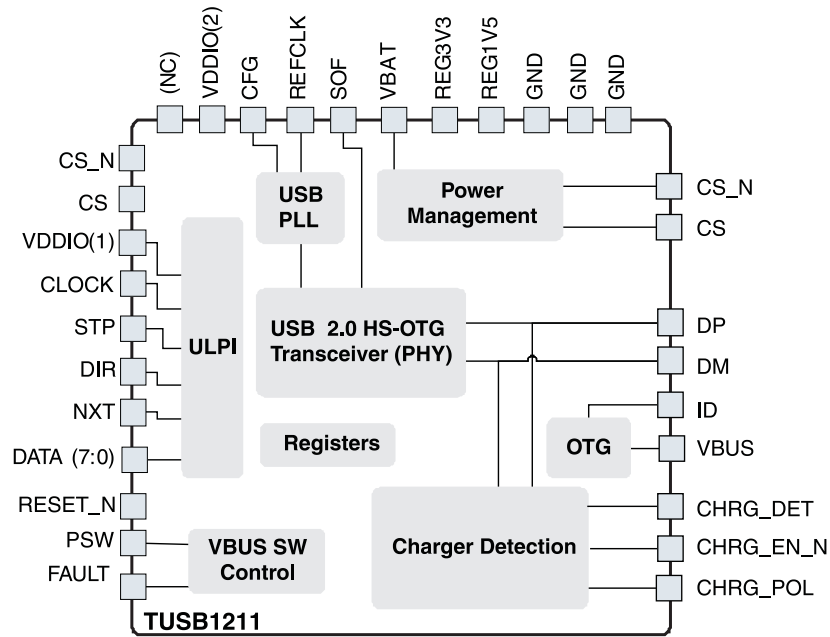
(4) LEVEL = Pin power supply level



**Table 2-1. Terminal Functions (continued)**

| #  | PIN <sup>(1)</sup> | NAME     | A/D <sup>(2)</sup> | TYPE <sup>(3)</sup> | LEVEL <sup>(4)</sup> | DESCRIPTION  |
|----|--------------------|----------|--------------------|---------------------|----------------------|--|
| 35 | F2                 | CHRG_DET | D                  | O                   | V <sub>BAT</sub>     | When CHRG_POL pin is at GND then CHRG_DET is in active low open-drain mode with external RCHRGDET (100K) connected to VBAT. When CHRG_POL pin is at VBAT then CHRG_DET is in active high open-source mode with external RCHRGDET (100K) connected to GND. This pin is 5V tolerant. |
| 36 | D4                 | PSW      | D                  | O                   | V <sub>BAT</sub>     | Controls an external, active high, VBUS power switch or charge pump. Open source output on VBAT supply when PSW_OSOD bit is 0 (default), open-drain active-low output when PSW_OSOD bit is 1. Requires an external RPSW (100K) pull down/up resistor to GND/VBAT .                 |

**2.2 Block Diagram**



### 3 Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

| PARAMETER         |  | CONDITIONS   | MIN  | MAX                       | UNIT |
|-------------------|--|--|------|---------------------------|------|
| V <sub>BAT</sub>  | Main battery supply voltage  | Continuous   | 0    | 5.0                       | V    |
|                   | Main battery supply voltage pulsed   | The product will have negligible reliability impact for pulsed voltage spikes of 5.5 V for a total (cumulative over lifetime) duration of 5 milliseconds |      | 5.5                       | V    |
| V <sub>DDIO</sub> | IO supply voltage  | Continuous   |      | 1.98                      | V    |
|                   | Voltage on any input except V <sub>DDIO</sub> , V <sub>BAT</sub> , and V <sub>BUS</sub> pads | Where V <sub>DD</sub> represents the voltage applied to the power supply pin associated with the input   | -0.3 | 1.0*V <sub>DD</sub> + 0.3 | V    |
|                   | DP, DM, ID high voltage short circuit  | DP or DM or ID pins short circuited to V <sub>BUS</sub> supply, in any mode of TUSB1211 operation, continuously for 24hours                              |      | 5.25                      | V    |
|                   | DP, DM, ID low voltage short circuit   | DP or DM or ID pins short circuited to GND in any mode of TUSB1211 operation, continuously for 24hours   | 0    |                           | V    |
|                   | V <sub>BUS</sub> input   |  | -2   | 20                        | V    |
| T <sub>stg</sub>  | Storage temperature range  |  | -55  | 125                       | °C   |
| T <sub>A</sub>    | Ambient temperature range  |  | -40  | 85                        | °C   |
| T <sub>J</sub>    | Junction temperature range   | Absolute maximum rating  | -40  | 150                       | °C   |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 3.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER             |   | TEST CONDITIONS  | MIN  | TYP | MAX  | UNIT |
|-----------------------|---|--|------|-----|------|------|
| V <sub>BAT</sub>      | Battery supply voltage  | VBAT_ACTIVE  | 2.7  | 3.6 | 4.8  | V    |
| V <sub>BAT_CERT</sub> | Battery supply voltage for USB 2.0 compliancy (USB 2.0 certification) | When V <sub>DD33</sub> is supplied internally                    | 3.15 |     |      | V    |
|                       |   | When V <sub>DD33</sub> is shorted to V <sub>BAT</sub> externally | 3.05 |     |      |      |
| V <sub>BAT_DB</sub>   | Battery supply voltage for charger detect in “dead-battery condition” | VBAT_DB  | 2.4  |     |      | V    |
| V <sub>DDIO</sub>     | IO supply voltage   | VDDIO_ACTIVE   | 1.62 | 1.8 | 1.95 | V    |
| T <sub>A</sub>        | Ambient temperature range   |  | -40  |     | 85   | °C   |
| T <sub>J</sub>        | Junction temperature  | For parametric compliance  | -40  |     | 125  | °C   |

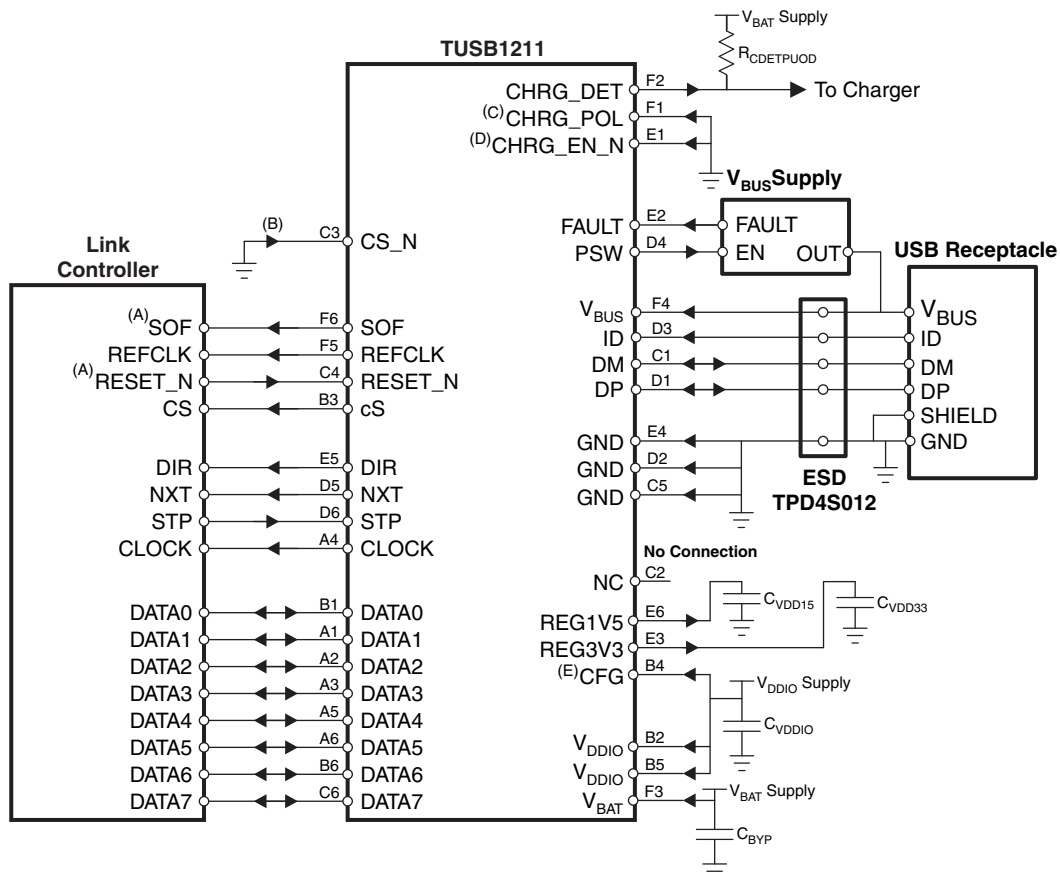
#### 3.3 ESD Electrical Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER |   | TEST CONDITIONS | MIN | TYP | MAX  | UNIT |
|-----------|---|-----------------|-----|-----|------|------|
| CDM       | Charged-Device Model stress voltage (JESD22-C101-A) | All pads        |     |     | 500  | V    |
| HBM       | Human-Body Model stress voltage (JESD22-A114D)      | All pads        |     |     | 2000 | V    |

## 4 Application Diagram

Figure 4-1 shows the suggested application diagram (Host or OTG, ULPI output-clock mode)



- Optional: SOF (open if unused); RESET\_N (tie to V<sub>DDIO</sub> if unused)
- Link controls chip select via CS pin with CS\_N at GND. Alternatively, Link may control CS\_N pin with CS pin tied to V<sub>DDIO</sub>.
- CHRG\_DET is active-low (tie CHRG\_POL to V<sub>BAT</sub> for CHRG\_DET active high).
- Dead battery charger detection is enabled (tie CHRG\_EN\_N to V<sub>BAT</sub> to disable).
- CFG tied to V<sub>DDIO</sub> for 26 MHz input at REFCLK (tie to GND for 19.2 MHz).

Figure 4-1. USB-OTG with ULPI Output Clock

## 5 Clock System

### 5.1 USB PLL Reference Clock

The USB PLL block generates the clocks used to synchronize:

- the ULPI interface (60 MHz clock)
- the USB interface (depending on the USB data rate, 480 Mbps, 12 Mbps or 1.5 Mbps)

TUSB1211 requires an external reference clock which is used as an input to the 480MHz USB PLL block. Depending on the clock configuration, this reference clock can be provided either at REFCLK pin or at CLOCK pin.

By default CLOCK pin is configured as an input.

Two clock configurations are possible:

- Input clock configuration (see [Section 5.1.1](#))
- Output clock configuration (see [Section 5.1.1](#))

#### 5.1.1 ULPI Input Clock Configuration

In this mode REFCLK must be externally tied to GND.

CLOCK remains configured as an input.

When the ULPI interface is used in “input clock configuration”, i.e., the 60 MHz ULPI clock is provided to TUSB1211 on CLOCK pin, then this is used as the reference clock for the 480 MHz USB PLL block.

**Table 5-1. Electrical Characteristics: CLOCK Input**

| PARAMETER                                  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT   |
|--|--|-----|-----|-----|--------|
| CLOCK input duty cycle                     |  | 40  |     | 60  | %      |
| F <sub>CLOCK</sub> CLOCK nominal frequency |  |     | 60  |     | MHz    |
| CLOCK input rise/fall time                 | In % of CLOCK period T <sub>CLOCK</sub> ( = 1/F <sub>CLOCK</sub> ) |     |     | 10  | %      |
| CLOCK input frequency accuracy             |  |     |     | 250 | ppm    |
| CLOCK input integrated jitter              |  |     |     | 600 | ps rms |

#### 5.1.2 ULPI Output Clock Configuration

In this mode a reference clock must be externally provided on REFCLK pin.

When an input clock is detected on REFCLK pin then CLOCK will automatically change to an output, i.e., 60 MHz ULPI clock is output by TUSB1211 on CLOCK pin.

Two reference clock input frequencies are supported. REFCLK input frequency is communicated to TUSB1211 via a configuration pin, CFG, see F<sub>REFCLK</sub> in [Table 5-2](#) for frequency correspondence.

TUSB1211 supports square-wave reference clock input only.

**Table 5-2. Electrical Characteristics: REFCLK**

| PARAMETER                                    | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT   |
|--|---|-----|------|-----|--------|
| REFCLK input duty cycle                      |   | 40  |      | 60  | %      |
| F <sub>REFCLK</sub> REFCLK nominal frequency | When CFG pin is tied to GND   |     | 19.2 |     | MHz    |
|  | When CFG pin is tied to V <sub>DDIO</sub>                             |     | 26   |     |        |
| REFCLK input rise/fall time                  | In % of REFCLK period T <sub>REFCLK</sub> ( = 1/F <sub>REFCLK</sub> ) |     |      | 20  | %      |
| REFCLK input freq accuracy                   |   |     |      | 250 | ppm    |
| REFCLK input integrated jitter               |   |     |      | 600 | ps rms |



## 6 Power Management

This chapter describes the electrical characteristics of the voltage regulators and timing characteristics of the supplies digitally controlled within the TUSB1211.

### 6.1 Power Provider

**Table 6-1. Summary of Internal Power Providers<sup>(1)</sup>**

| SUPPLY NAME | PIN NAME | TYPE | TYPICAL VOLTAGE (V) |
|-------------|----------|------|---------------------|
| REG1V5      | REG1V5   | LDO  | 1.5                 |
| REG1V8      | -        | LDO  | 1.8                 |
| REG3V3      | REG3V3   | LDO  | 3.1                 |

(1) REG3V3 may be supplied externally, or by shorting the REG3V3 pin to VBAT pin provided VBAT min is in range [3.2 V : 3.6 V]. Note that the REG3V3 LDO will always power-on when the chip is enabled, irrespective of whether VDD33 is supplied externally or not.

### 6.2 Power Consumption

Table 6-2 describes the power consumption depending on the use cases.

Typical power consumption is obtained in nominal operating conditions of TUSB1211.

**Table 6-2. Power Consumption**

| MODE        | CONDITIONS  | SUPPLY      | TYPICAL POWER CONSUMPTION | UNIT          |
|-------------|---|-------------|---------------------------|---------------|
| OFF         | $V_{BAT} = 3.6\text{ V}$ , $V_{DDIO} = 1.8\text{ V}$ ,<br>$CS = 0\text{ V}$   | $I_{VBAT}$  | 8                         | $\mu\text{A}$ |
|             |   | $I_{VDDIO}$ | 1.8                       |               |
|             |   | $I_{TOTAL}$ | <b>9.8</b>                |               |
| Suspend     | $V_{BUS} = 5\text{ V}$ , $V_{BAT} = 3.6\text{ V}$ ,<br>$V_{DDIO} = 1.8\text{ V}$ , $V_{CHRG\_EN\_N} = 0\text{ V}$ ,<br>no clock | $I_{VBAT}$  | 251                       | $\mu\text{A}$ |
|             |   | $I_{VDDIO}$ | 21                        |               |
|             |   | $I_{TOTAL}$ | <b>272</b>                |               |
| HS USB Mode | $V_{BAT} = 3.6\text{ V}$ , $V_{DDIO} = 1.8\text{ V}$ ,<br>active USB transfer   | $I_{VBAT}$  | 46.4                      | mA            |
|             |   | $I_{VDDIO}$ | 1.3                       |               |
|             |   | $I_{TOTAL}$ | <b>47.7</b>               |               |
| FS USB Mode | $V_{BAT} = 3.6\text{ V}$ , $V_{DDIO} = 1.8\text{ V}$ ,<br>active USB transfer   | $I_{VBAT}$  | 31.4                      | mA            |
|             |   | $I_{VDDIO}$ | 1.3                       |               |
|             |   | $I_{TOTAL}$ | <b>32.7</b>               |               |

### 6.3 Power Control

#### 6.3.1 Overview

TUSB1211 can be powered up in two different modes:

- Standard power-up condition

For this,  $V_{BAT}$  and  $V_{IO}$  must be present and chip must be selected ( $CS=1$  and  $CS\_N=0$ ). See 9.3.3.1 Standard Power-up Timing Power resources will be configured sequentially until the device reaches the power state.

USBON . At this time internal power-on-reset signal PORZ will be released and USB PLL will start up. Once PLL is locked, the DIR output pin will be deasserted allowing TUSB1211 to be configured by the USB Link Controller via the ULPI interface.

Note that by default TUSB1211 will be configured as a Host not providing VBUS as required by

register map in ULPI specification Rev1.1.

This is the case because OTG\_CONTROL register bits DRVVBUS and DRVVBUSEXTERNAL bits are 0 by default, and DPPULLDOWN, DMPULLDOWN bits are 1 by default such that the 15 k $\Omega$  pulldown resistors at DP/DM pins are enabled by default.

It is the responsibility of the link to enable external VBUS supply if required in Host mode, or to reconfigure the PHY if required in Device mode.

- Hardware charger detection power-up

When the chip is not selected (CS=0 or CS\_N=1), but VBUS is present and CHRG\_EN\_N pin is at GND, and VBAT > VBAT\_MNTR then TUSB1211 will power-up in Hardware Charger Detection Mode.

Power resources will be configured sequentially until the device reaches the power state USBON . However since chip is not selected, internal power-on-reset signal PORZ will be not be released and USB PLL will not start up. Instead the device will enter USB Battery charger finite state machine (FSM) .

## 7 USB Transceiver (PHY)

The TUSB1211 device includes a universal serial bus (USB) on-the-go (OTG) transceiver that supports USB 480 Mb/s high-speed (HS), 12 Mb/s full-speed (FS), and USB 1.5 Mb/s low-speed (LS) through a 12-pin UTMI+ low pin interface (ULPI).

### NOTE

LS device mode is not allowed by a USB2.0 HS capable PHY, therefore it is not supported by TUSB1211. This is clearly stated in USB2.0 standard Chapter 7, page 119, second paragraph: “A *high-speed capable upstream facing transceiver must not support low-speed signaling mode.*” There is also some related commentary in Chapter 7.1.2.3.

**Table 7-1. Interface Target Frequencies**

| IO INTERFACE | INTERFACE DESIGNATION | TARGET FREQUENCY |             |
|--------------|-----------------------|------------------|-------------|
| USB          | Universal serial bus  | High speed       | 480 Mbits/s |
|              |                       | Full speed       | 12 Mbits/s  |
|              |                       | Low speed        | 1.5 Mbits/s |

### 7.1 PHY Overview

The PHY is the physical signaling layer of the USB 2.0. It essentially contains all the drivers and receivers required for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces to the USB controller through a standard 12-pin digital interface called UTMI+ low pin interface (ULPI).

The transmitters and receivers inside the PHY are classified into two main classes.

- The full-speed (FS) and low-speed (LS) transceivers. These are the legacy USB1.x transceivers.
- The HS (HS) transceivers

In order to bias the transistors and run the logic, the PHY also contains reference generation circuitry which consists of:

- A PLL which does a frequency multiplication to achieve the 480-MHz low-jitter clock necessary for USB and also the clock required for the switched capacitor resistance block.
- Internal biasing circuitry

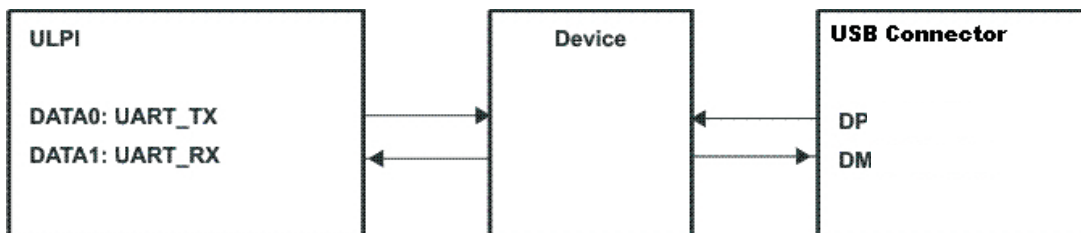
Built-in pullup and pulldown resistors are used as part of the protocol signaling.

Apart from this, the PHY also contains circuitry which protects it from accidental short on the DP and DM lines to 5 V or GND.



## 8 UART Transceiver

By setting CARKITMODE bit in IFC\_CTRL register TUSB1211 will enter UART mode. In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter at DM pin and receiver at DP pin.



**Figure 8-1. USB UART Data Flow**

## 9 USB On-The-Go (OTG) Feature

The on-the-go (OTG) block integrates two main functions:

- ID resistor detection including Accessory Charger Adapter (ACA) detection
- $V_{BUS}$  level detection and SRP pullup/pulldown resistors

## 10 USB Battery Charger Detection and ACA Feature

In order to support Battery Charging Specification v1.1 April 2009 [BCS v1.1], a charger detection module is included inside TUSB1211 module.

This feature includes:

- Battery charger detection sensing and control on DP/DM lines
- ACA (Accessory Charger Adapter) detection and control on ID line

The detection mechanism aims at distinguishing several types of power sources that can be connected on VBUS line:

- Dedicated Charging Port
- Standard Downstream Port
- Charging Downstream Port

Hardware includes:

- a dedicated voltage referenced pullup on DP line
- a dedicated current controlled pulldown on DM line
- a detection comparator on DM line - a control/detection finite state machine (FSM) including timers
- a charger detection output pin (CHRG\_DET) for external charger control
- detection comparators on ID line

ID pin status detection (as defined per OTG v1.3 standard as well as ACA resistor types as described in BCS v1.1) and DP/DM Single-Ended receivers (as defined per USB v2.0 standard) are also used to determine the type of device plugged on USB connector.

USB charger detection is an independent feature, on  $V_{BAT}$  supply domain, using CK32K clock.

### 10.1 USB Battery Charger Detection Modes



There are 3 modes of operation of battery charger detection module:

1. Hardware Charger Detection Module
2. Software Mode
3. Software FSM Mode

### 10.2 Accessory Charger Adapter (ACA) Detection

Accessory Charger Adapter (ACA) feature is defined in the USB Battery Charging Specification Rev. 1.1 specification. ACA allows simultaneous connection of a USB Charger or Charging Downstream Port and an Accessory to a portable OTG device (TUSB1211).via only a single USB OTG port.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type               | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples   |
|------------------|---------------|----------------------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|---|
| TUSB1211A1ZRQ    | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZRQ                | 36   | 490         | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-2-260C-1 YEAR  | -40 to 85    | 1211A1                   |  |
| TUSB1211A1ZRQR   | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZRQ                | 36   | 1500        | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-2-260C-1 YEAR  | -40 to 85    | 1211A1                   |  |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type         | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TUSB1211A1ZRQR | BGA MICROSTAR JUNIOR | ZRQ             | 36   | 1500 | 330.0              | 12.4               | 3.7     | 3.7     | 1.4     | 8.0     | 12.0   | Q1            |

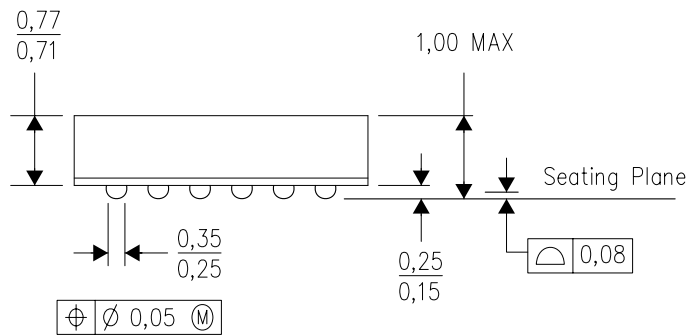
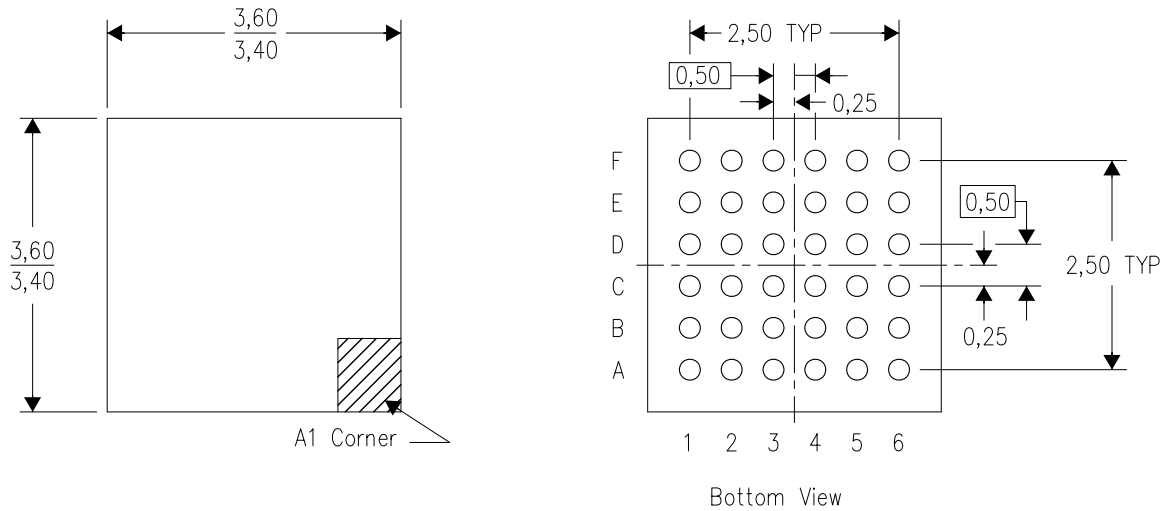
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type         | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| TUSB1211A1ZRQR | BGA MICROSTAR JUNIOR | ZRQ             | 36   | 1500 | 336.6       | 336.6      | 31.8        |

ZRQ (S-PBGA-N36)

PLASTIC BALL GRID ARRAY



4210358/A 07/09

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. This is a Pb-free solder ball design.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

|                              |  |
|------------------------------|--|
| Audio                        | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                               |
| Amplifiers                   | <a href="http://amplifier.ti.com">amplifier.ti.com</a>                               |
| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>   |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>   |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |  |
|-------------------------------|--|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)