CT2 I/Q Modulator and Clock Circuitry

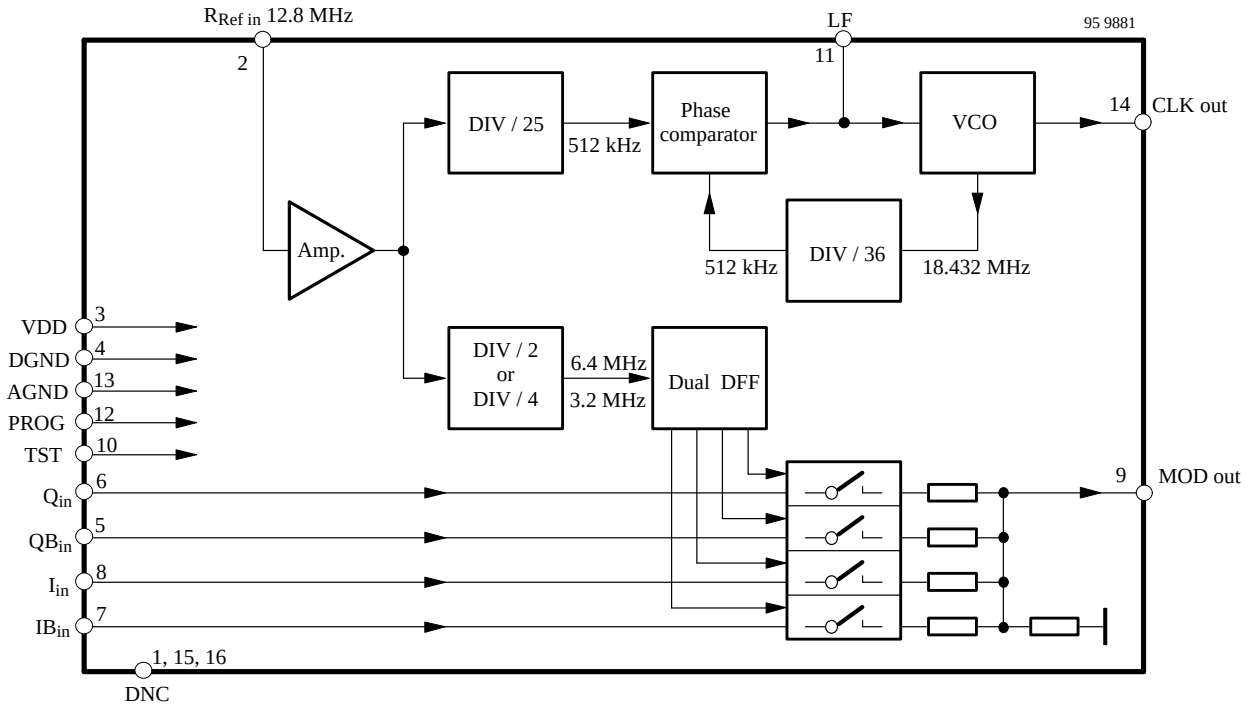
Description

U3770M is a quadrature modulator realized with MATRA MHS' advanced 0.8 micron CMOS process. The IC is especially designed for CT2 application in con-junction with TELEFUNKEN's RF/IF signal processor U2760B and a CT2 baseband controller (i.e., AMD PhoX^{TM} controller Am79C4xx). Together with TELEFUNKEN's PLL IC U2783B and the GaAs front end U7001BG, a complete CT2 chip set is available.

Features

- Programmable 0.8/1.6 MHz quadrature modulated carrier generation
- More than 30 dB LO and sideband suppression
- 18.432 MHz CMOS level clock generation
- Supply voltage range 2.7 to 3.3 V
- Low power consumption, typical 6 mW
- SO16 package or die form

Block Diagram



Functional Description

U3770M has been designed to reduce power consumption and cost of CT2 devices. An innovative CMOS I,Q modulator with an extremely low current provides all the advantages of I,Q modulation:

– No requirement for FM deviation tuning

– Eliminates the Gaussian filter

– Simplifies the power ramping control

The modulated output carrier can be programmed to be 0.8 MHz or 1.6 MHz by the PROG control pin.

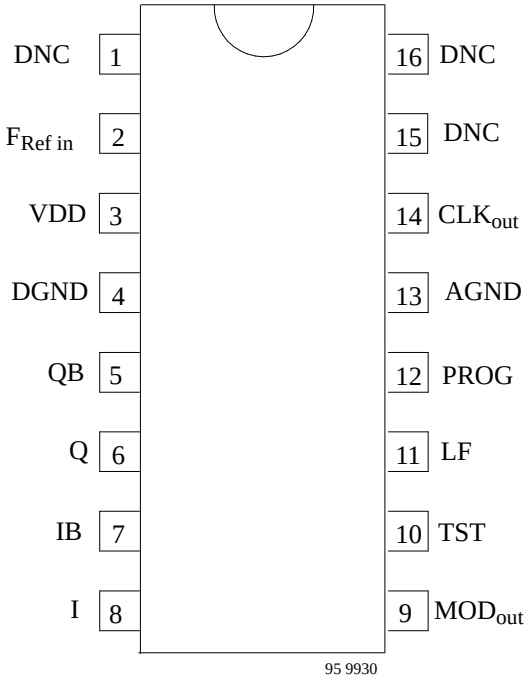
The typical supply voltage is 3 V @ 2 mA.

To reduce overall system cost, an internal PLL generates a 18.432 MHz clock signal from the system 12.8 MHz reference oscillator. This way, only one crystal oscillator is needed in the complete CT2 device.

Internally, the 12.8 MHz reference signal is fed into a shaping amplifier and then into two logic dividers, to generate a 512 kHz and a programmable 3.2 or 6.4 MHz clock. This clock is divided by 4 by two D flip-flops. The flip-flop outputs drive the four analog switches in quadrature. A pair of analog switches make a local oscillator (LO) suppression mixer. By summing the other pair outputs, we obtain both LO and sideband suppression, of more than –30 dBc.

The 512 kHz clock drives a frequency synthesizer. The VCO runs at a fixed frequency of 18.432 MHz. The VCO control voltage (LF pin) controls the VCO frequency.

Pin Description



Pin	Symbol	Function
2	$F_{Ref\ in}$	External 12.8 MHz reference frequency input
3	VDD	Supply voltage
4	DGND	Digital ground
5	QB_{in}	Analog switches input
6	Q_{in}	Analog switches input
7	IB_{in}	Analog switches input
8	I_{in}	Analog switches input
9	MOD_{out}	Modulator output signal
10	TST	Test input, must be connected to GND (only factory use)
11	LF	PLL loop filter
12	PROG	PROG = 0, 1.6 MHz mode PROG = 1, 0.8 MHz mode
13	AGND	Analog ground
14	CLK_{out}	Digital CMOS clock output 18.432 MHz
1, 15, 16	DNC	Do not connect

Absolute Maximum Ratings

Stresses at or above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD}	6	V
Modulator input voltages	I IB Q QB	–0.5 to V_{DD}	V
Reference frequency input	$F_{Ref\ in}$	–0.5 to V_{DD}	V
Ambient temperature	T_{amb}	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C
Junction temperature	T_j	$T_j < T_{amb}$ +10	°C

Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD}	3 ± 10%	V
Ambient temperature	T_{amb}	–5 to +70	°C
Junction temperature	T_j	$T_j < T_{amb}$ +5	°C
Storage temperature	T_{stg}	–40 to +125	°C

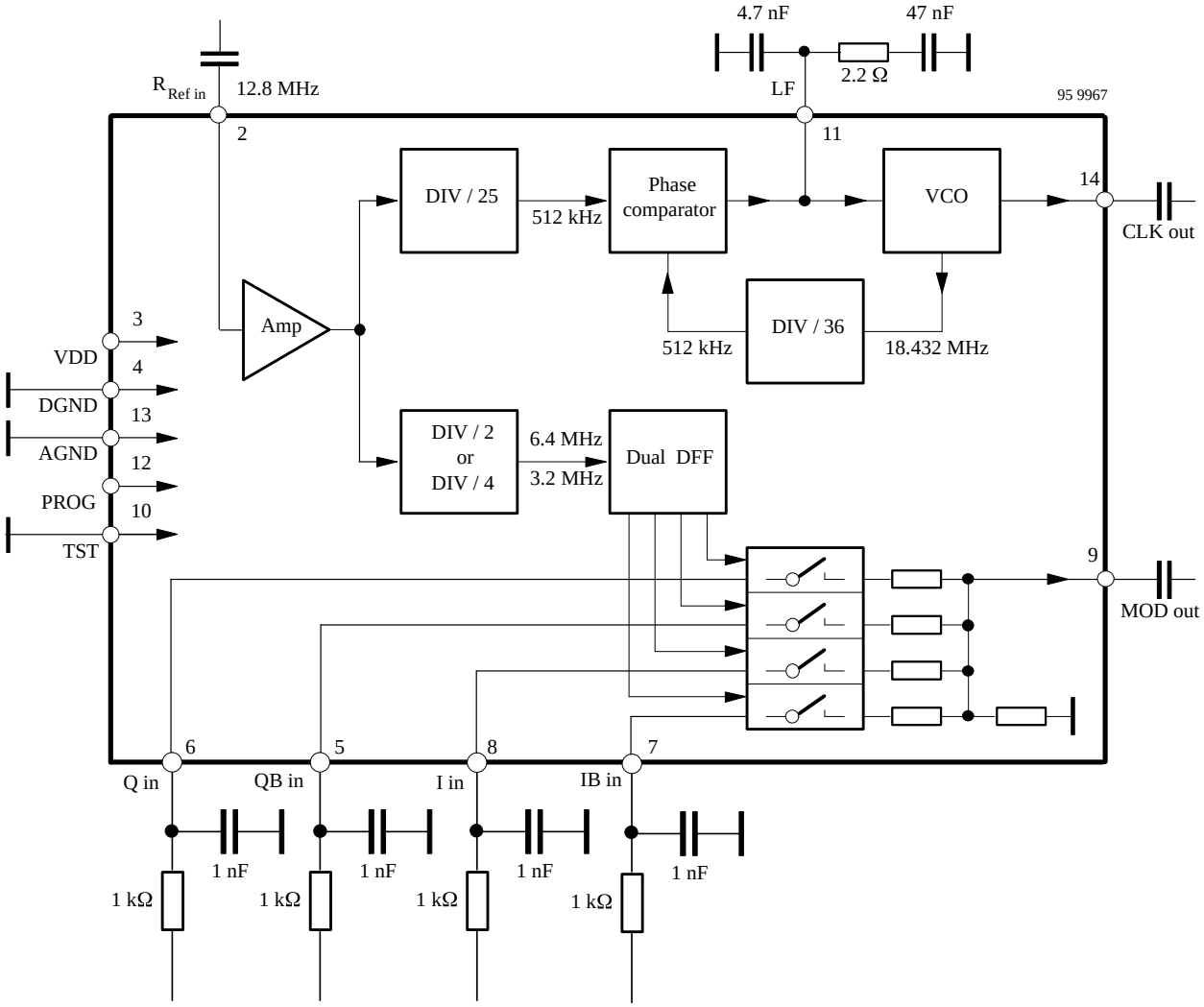
Electrical Characteristics

Test conditions (unless otherwise specified) related to test circuit
V_S = 3 V, V_{BIi}, $V_{\overline{BI}i}$ and V_{BQi}, $V_{\overline{BQ}i}$ = 1 V_{PP} single ended, oscillator frequency $F_{Ref\ in}$ = 12.8 MHz, T_{amb} = –5 to +70°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pin 3	V_{DD}	2.7	3	3.3	V
Supply current [1]	Pin 3	I_{DD}		2		mA
$F_{Ref\ in}$	Pin 2					
Input voltage		$V_{F\ Ref\ in}$	150			mV_{PP}
Input impedance		$Z_{F\ Ref\ in}$	100			kΩ
I, Q inputs	Pins 5, 6, 7 and 8					
Input voltage	Single ended	$V_{Iin,\ Qin}$		1		V_{PP}
Input impedance	Single ended	$Z_{Iin,\ Qin}$		20		kΩ
Input frequency		$F_{Iin,\ Qin}$		18		kHz
External bias voltage		$V_{IB,\ QB}$		1.5		V
MOD_{out}	Pin 9					
Output level [2]	Unloaded	$V_{Mod\ out}$		70		mVRMS
LO and sideband suppression		LO sub SB sub		–30		dBc
Output impedance		$Z_{Mod\ out}$		5		kΩ
CLK_{out}	Pin 14					
Output frequency		$F_{CLK\ out}$		18.432		MHz
Output level		$V_{CLK\ out}$		CMOS		
Output load		$Z_{CLK\ out}$			50	pF

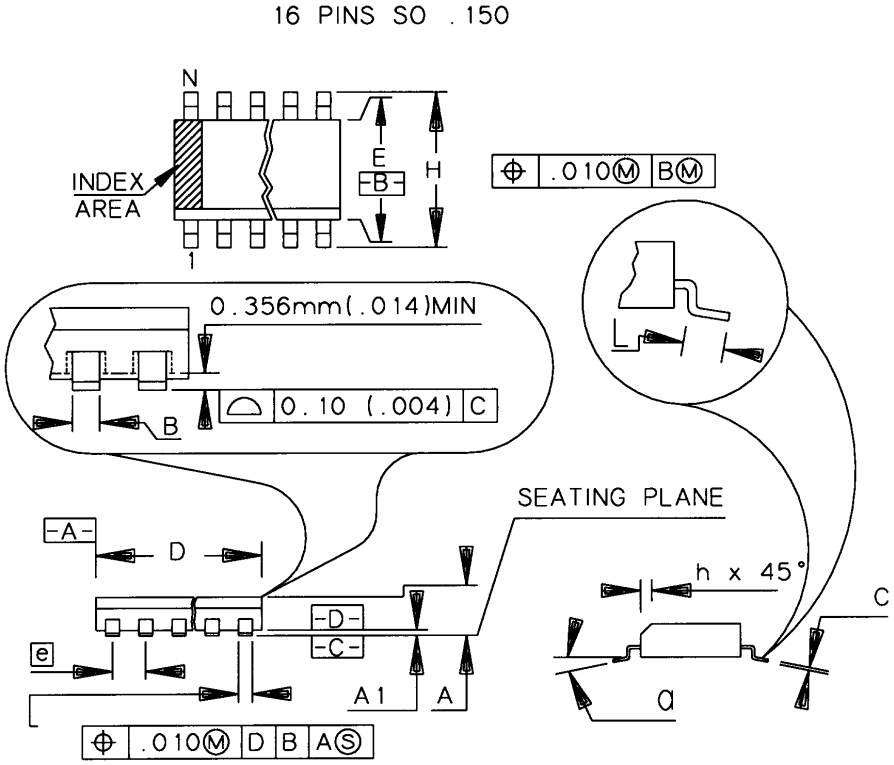
Note 1) C_L = 50 pF on Pin 14
Note 2) The output signal contains some harmonics, to be filtered by an external low-pass filter

Test Circuit



Dimensions in mm

Package: SO 16



	MM		INCH	
A	1.55	1.73	.061	.068
A1	0.127	0.25	.004	.0098
B	0.35	0.49	.014	.019
C	0.19	0.25	.0075	.0098
D	9.80	9.98	.386	.393
E	3.81	3.99	.150	.157
e	1.27	BSC	.050	BSC
H	5.84	6.20	.230	.244
h	0.25	0.41	.010	.016
L	0.41	0.89	.016	.035
N	16		16	
α	0°		8°	

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423