

SWITCHING
P-CHANNEL POWER MOS FFT
INDUSTRIAL USE

DESCRIPTION

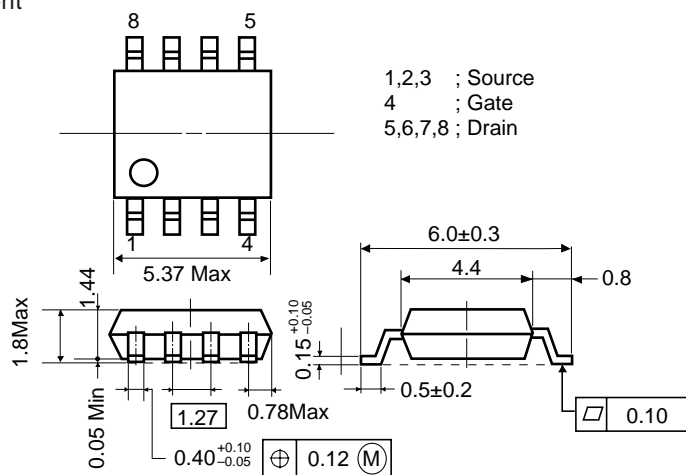
This product is P-Channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computers.

FEATURES

- Low On-Resistance
 $R_{DS(on)1} = 70 \text{ m}\Omega \text{ Max. (} V_{GS} = -10\text{V, } I_D = -2.5\text{A)}$
 $R_{DS(on)2} = 0.16 \Omega \text{ Max. (} V_{GS} = -4\text{V, } I_D = -2.0\text{A)}$
- Low C_{iss} $C_{iss} = 980\text{pF Typ.}$
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

PACKAGE DIMENSIONS

(in millimeter)



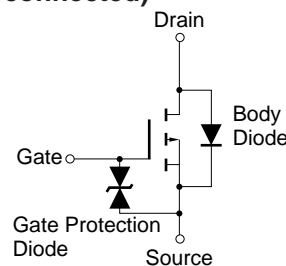
1,2,3 ; Source
4 ; Gate
5,6,7,8 ; Drain

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected)

Drain to Source Voltage	V_{DSS}	-30	V
Gate to Source Voltage	V_{GSS}	$\bar{+} 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\bar{+} 5.0$	A
Drain Current (pulse)*	$I_{D(pulse)}$	$\bar{+} 20$	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)** P_T		2.0	W
Channel Temperature	T_{ch}	150	C
Storage Temperature	T_{stg}	-50 to +150	C

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

** Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 0.7 \text{ mm}$



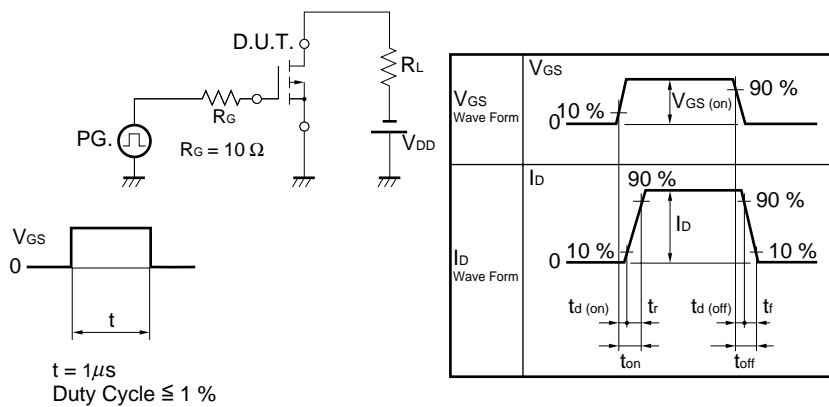
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

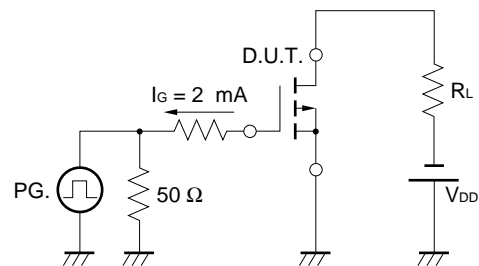
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = -10V, I _D = -2.5A		50	70	mΩ
	R _{DS(on)2}	V _{GS} = -4V, I _D = -2.0A		110	160	mΩ
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = -10V, I _D = -1mA	-1.0	-1.5	-2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = -10V, I _D = -2.5A	3.0	5.0		S
Drain Leakage Current	I _{DSS}	V _{DS} = -30V, V _{GS} = 0			-10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0			±10	μA
Input Capacitance	C _{iss}	V _{DS} = -10V		980		pF
Output Capacitance	C _{oss}	V _{GS} =0		780		pF
Reverse Transfer Capacitance	C _{rss}	f = 1MHz		430		pF
Turn-On Delay Time	t _{d(on)}	I _D = -2.5A		25		ns
Rise Time	t _r	V _{GS(on)} = -10V		80		ns
Turn-Off Delay Time	t _{d(off)}	V _{DD} = -15V		100		ns
Fall Time	t _f	R _G = 10Ω		100		ns
Total Gate Charge	Q _G	I _D = -5.0A		38		nC
Gate to Source Charge	Q _{GS}	V _{DD} = -24V		3.6		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = -10V		17		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 5.0A, V _{GS} = 0		0.8		V
Reverse Recovery Time	t _{rr}	I _F = 5.0A, V _{GS} = 0		85		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 50A/μs		200		nC

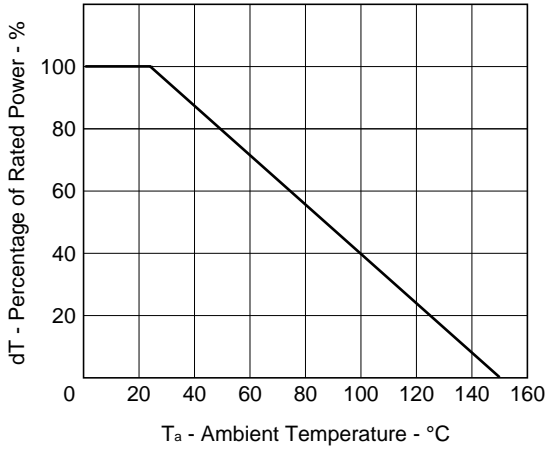
Test Circuit 1 Switching Time



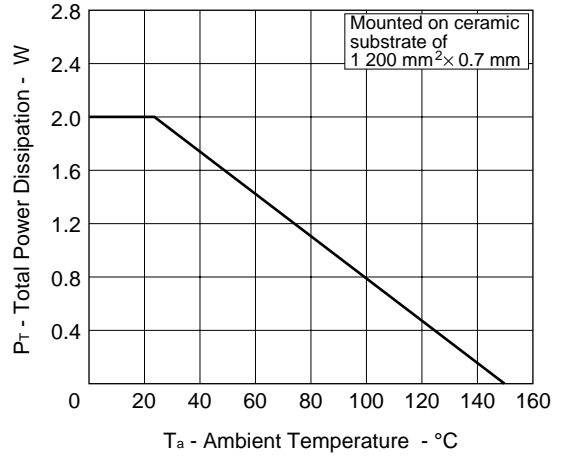
Test Circuit 2 Gate Charge



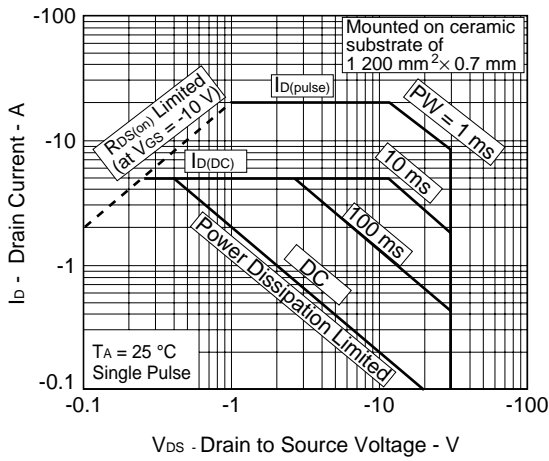
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



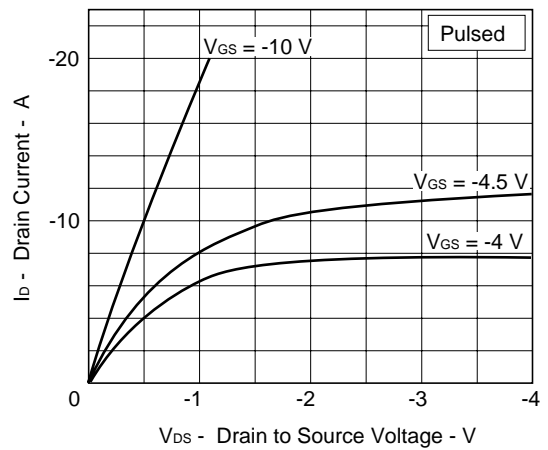
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



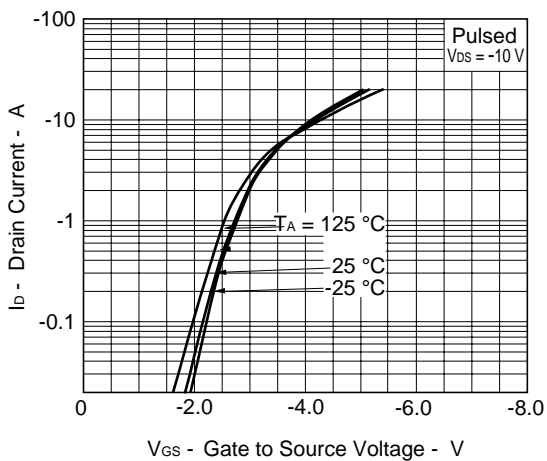
FORWARD BIAS SAFE OPERATING AREA



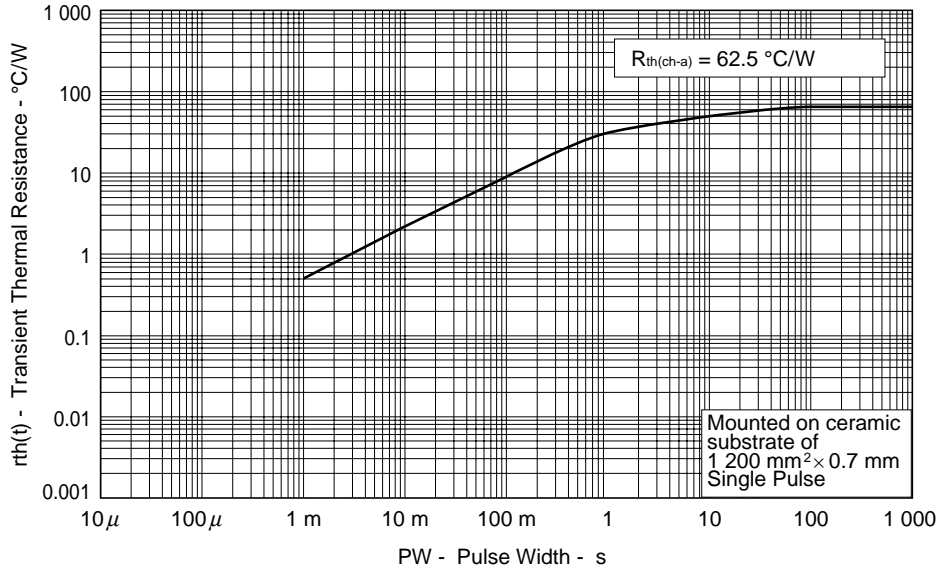
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



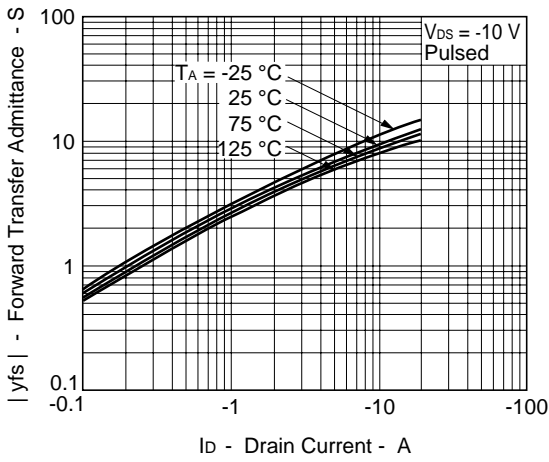
FORWARD TRANSFER CHARACTERISTICS



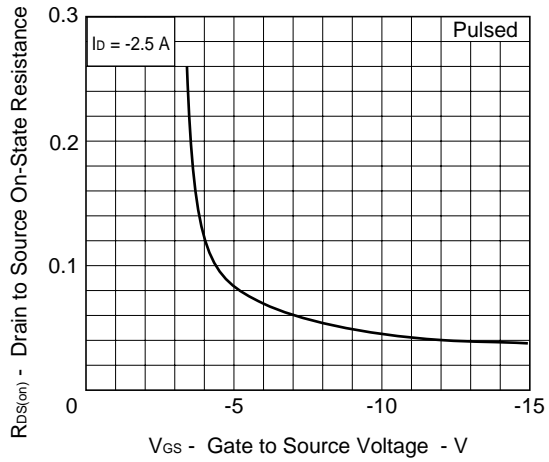
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



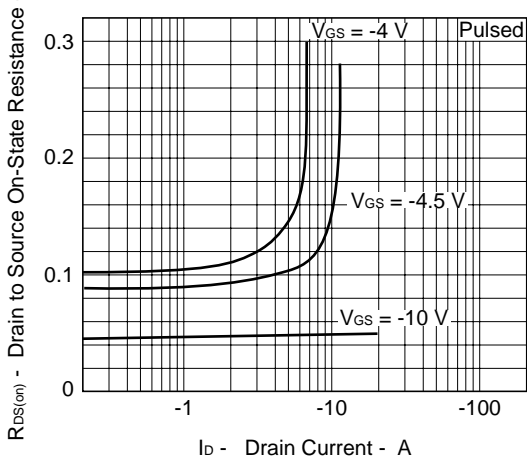
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



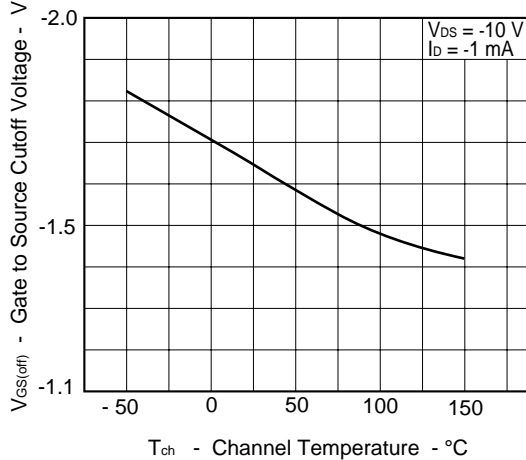
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

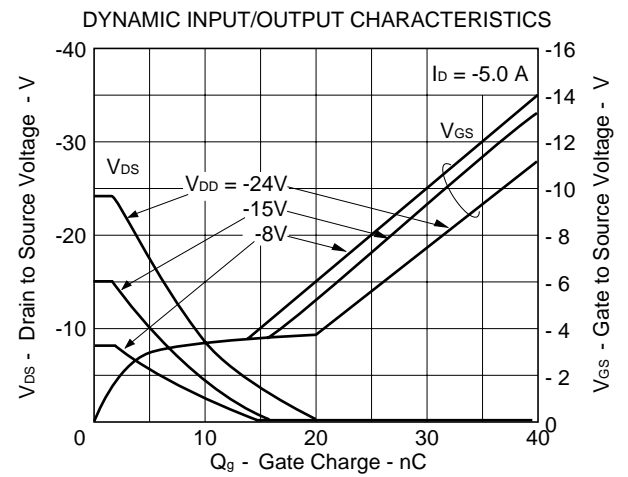
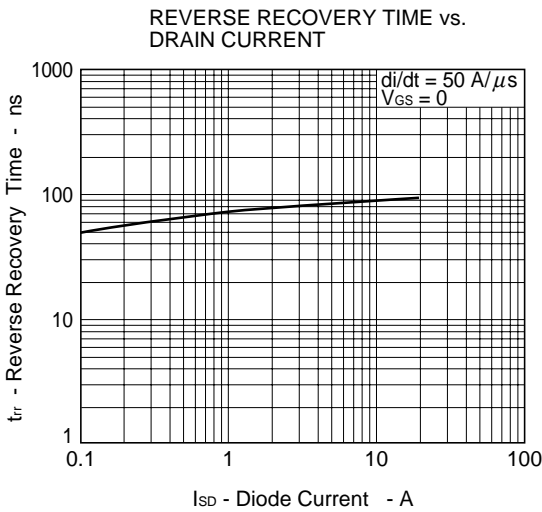
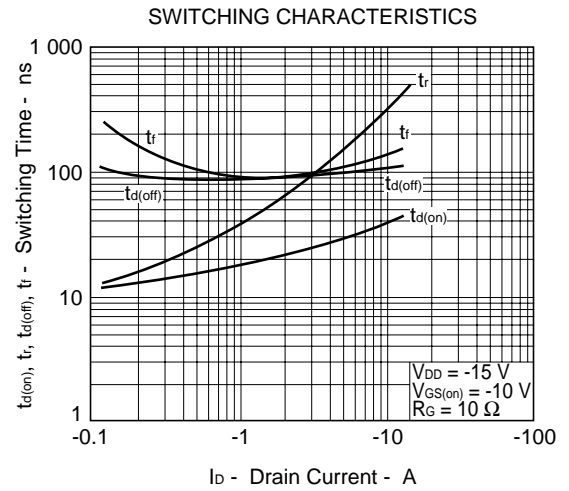
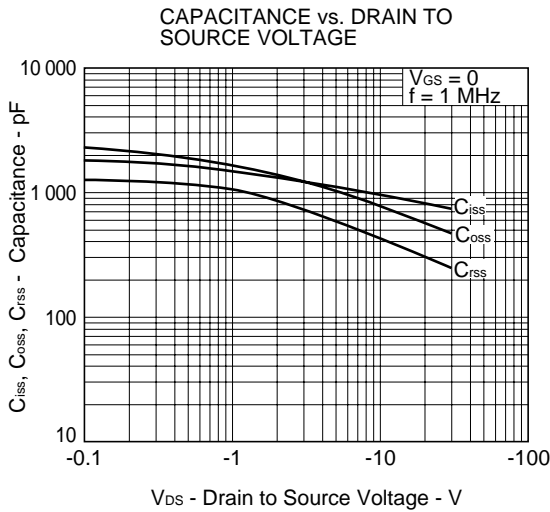
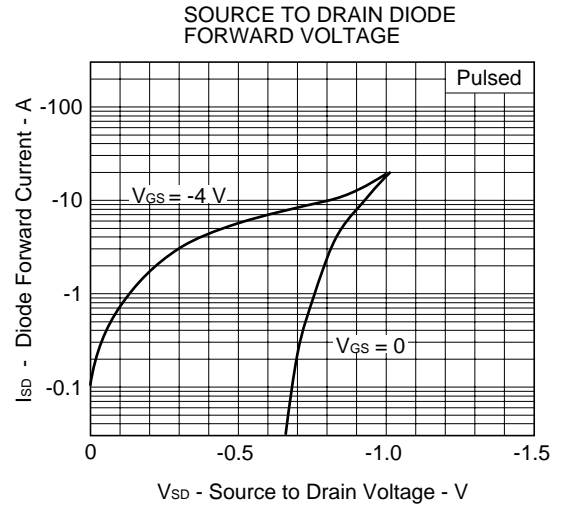
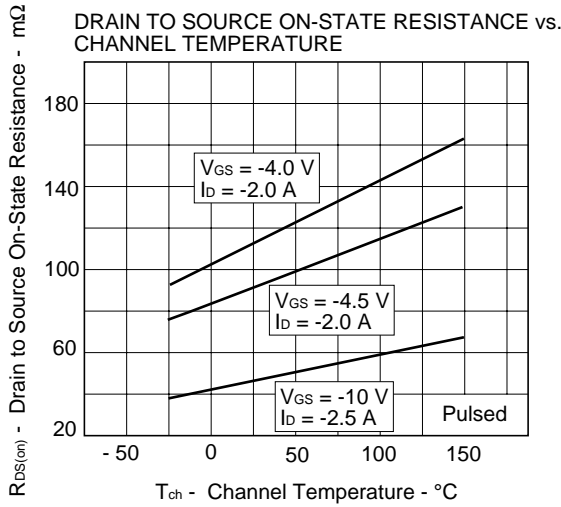


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.