NEC

MOS FIELD EFFECT TRANSISTOR
μPA1710A

SWITCHING
P-CHANNEL POWER MOS FET
INDUSTRIAL USE

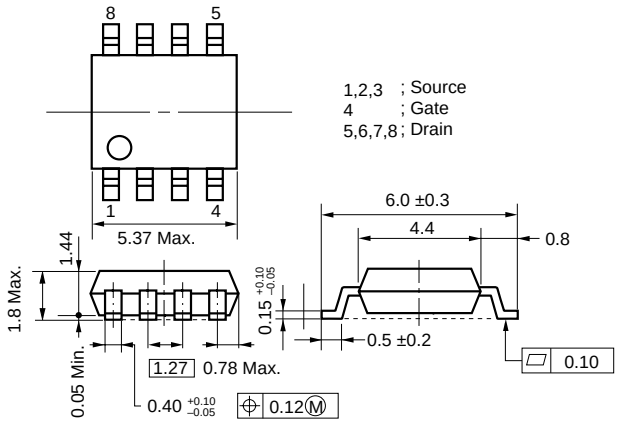
DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computers.

FEATURES

- Low on-resistance
  $R_{DS(on)1}$ = 70 mΩ (MAX.) (V_{GS} = –10 V, I_D = –2.5 A)
  $R_{DS(on)2}$ = 160 mΩ (MAX.) (V_{GS} = –4 V, I_D = –2.0 A)
- Low C_{iss} : C_{iss} = 840 pF (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



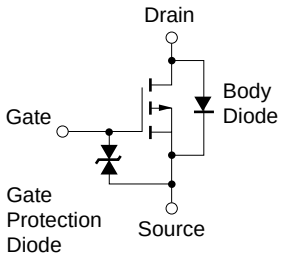
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1710AG	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±5.0	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±20	A
Total Power Dissipation (T_A = 25°C) Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C

EQUIVARENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Mounted on ceramic substrate of 1200 mm^2 x 1.1 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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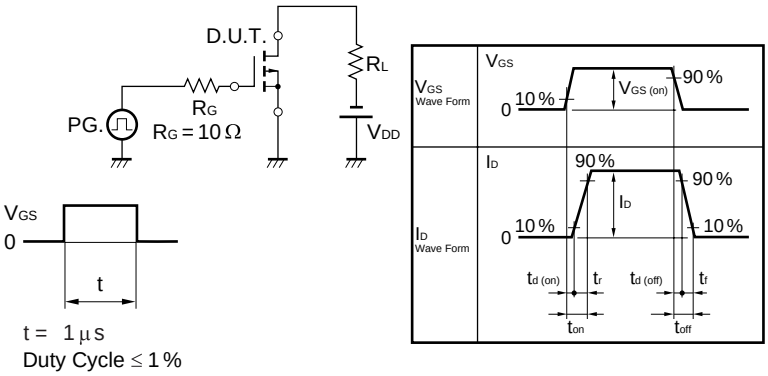
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

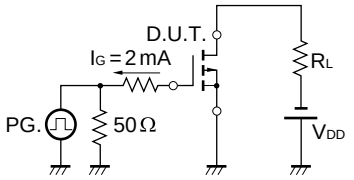
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –2.5 A		45	70	mΩ
	$R_{DS(on)2}$	V_{GS} = –4 V, I_D = –2.0 A		91	160	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0	–1.8	–2.5	V
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	V_{DS} = –10 V, I_D = –2.5 A	3.0	5.6		S
Drain Leakage Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = –10 V V_{GS} = 0 V f = 1 MHz		840		pF
Output Capacitance	C_{oss}			570		pF
Reverse Transfer Capacitance	C_{rss}			190		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = –2.5 A $V_{GS(on)}$ = –10 V V_{DD} = –15 V R_G = 10 Ω		13		ns
Rise Time	t_r			66		ns
Turn-off Delay Time	$t_{d(off)}$			82		ns
Fall Time	t_f			52		ns
Total Gate Charge	Q_G	I_D = –5.0 A V_{DD} = –24 V V_{GS} = –10 V		27.3		nC
Gate to Source Charge	Q_{GS}			2.7		nC
Gate to Drain Charge	Q_{GD}			8.2		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 5.0 A, V_{GS} = 0 V		0.81		V
Reverse Recovery Time	t_{rr}	I_F = 5.0 A, V_{GS} = 0 V di/dt = 50 A/μs		61		ns
Reverse Recovery Charge	Q_{rr}			71		nC

TEST CIRCUIT 1 SWITCHING TIME



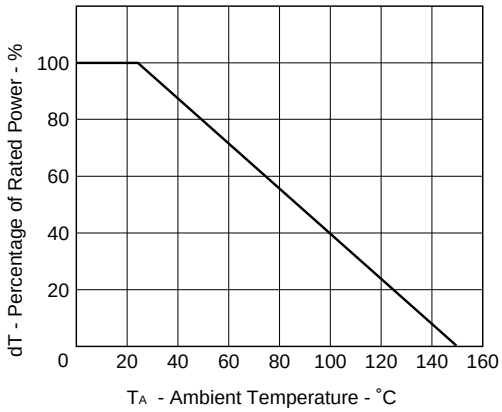
t = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

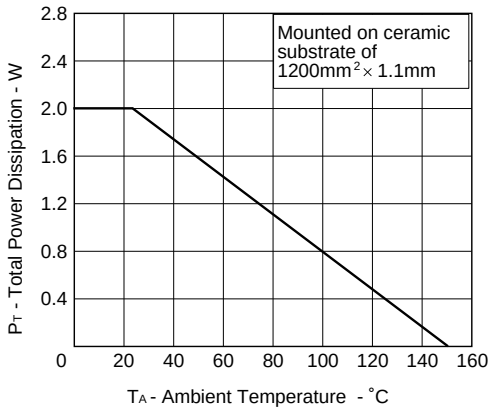


TYPICAL CHARACTERISTICS (T_A = 25 °C)

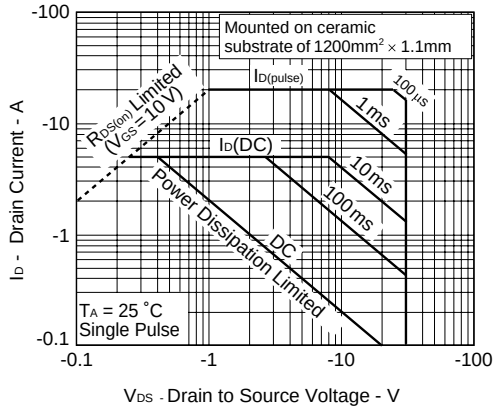
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



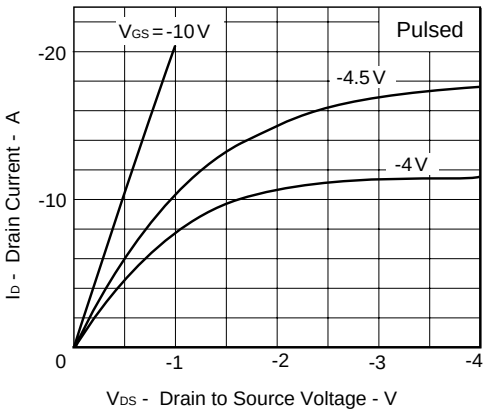
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



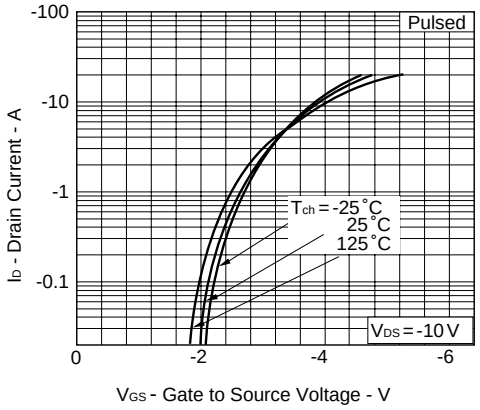
FORWARD BIAS SAFE OPERATING AREA



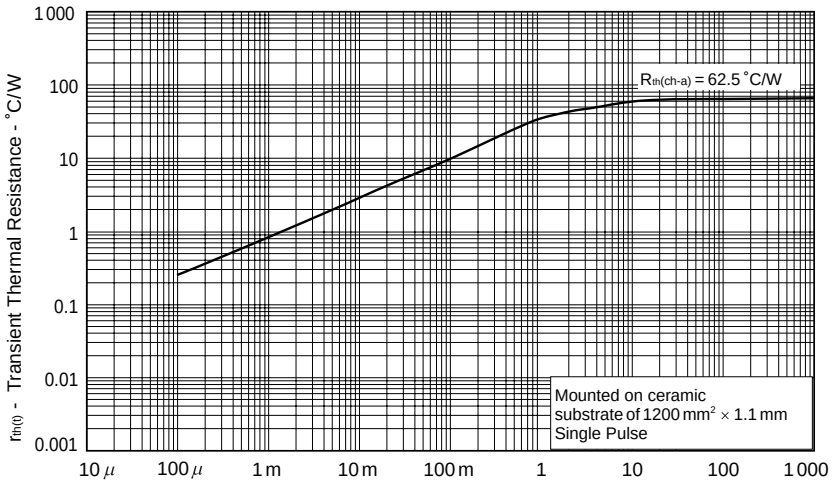
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



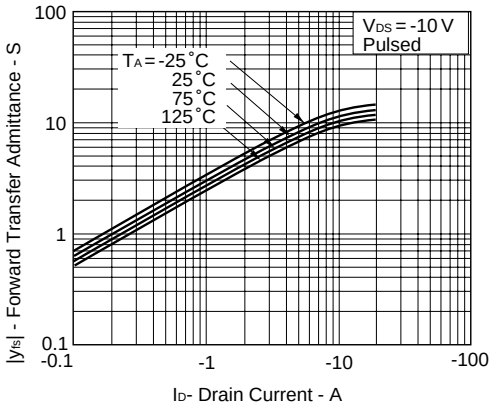
FORWARD TRANSFER CHARACTERISTICS



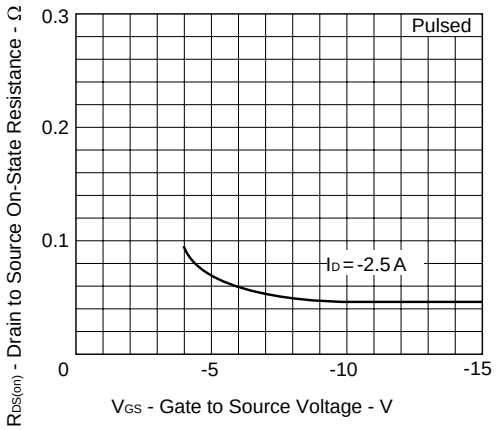
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



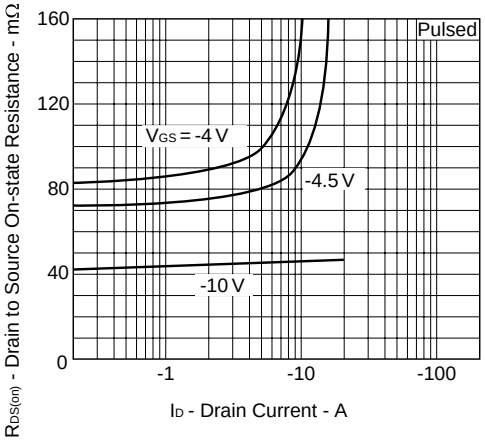
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



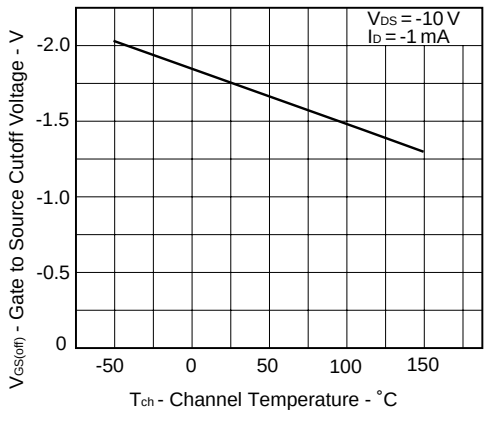
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



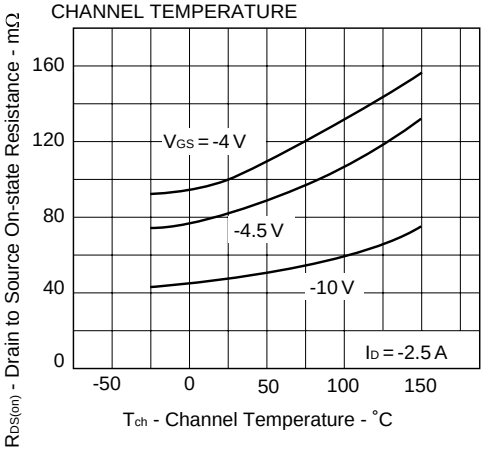
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



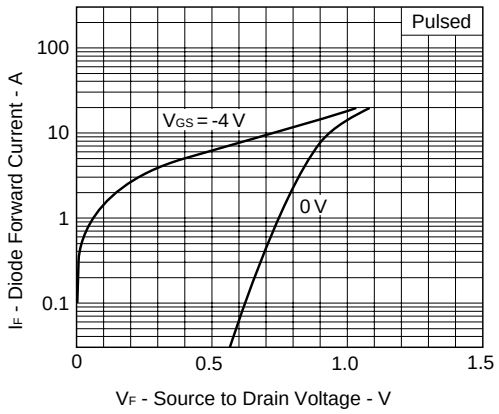
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



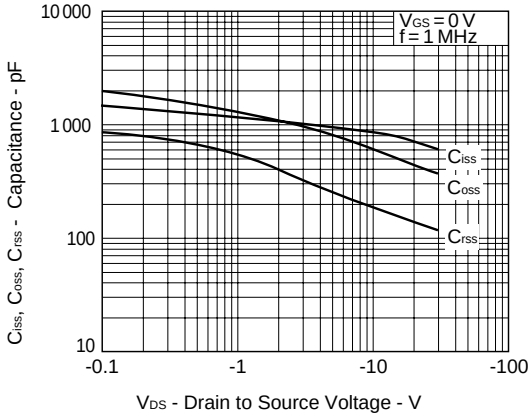
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



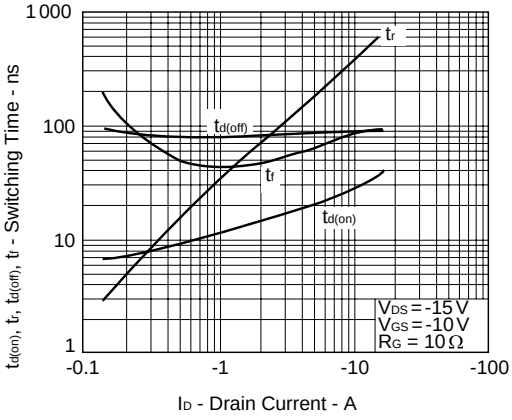
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



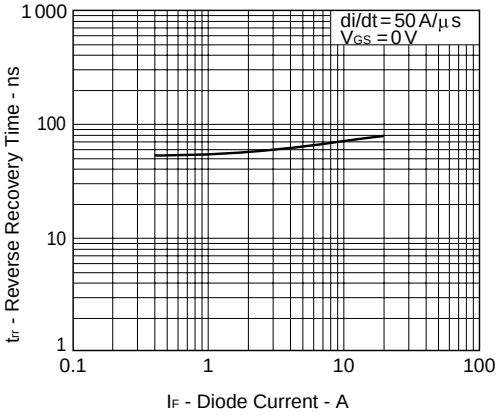
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



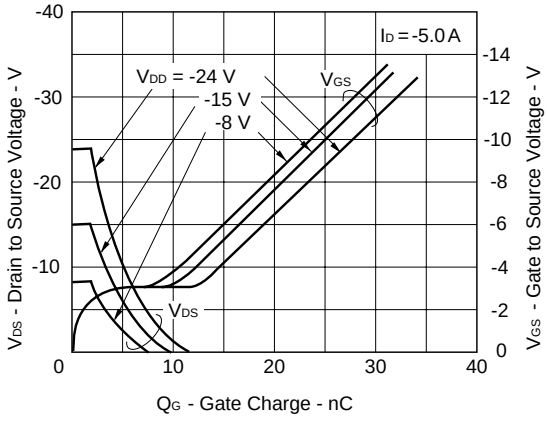
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



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