

MOS FIELD EFFECT TRANSISTOR

μ PA1710A

SWITCHING

P-CHANNEL MOS FET

INDUSTRIAL USE

DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computers.

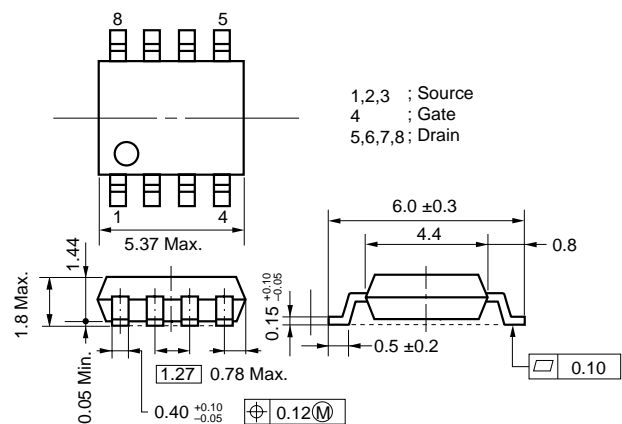
FEATURES

- Low on-resistance
 $R_{DS(on)1} = 70 \text{ m}\Omega$ (MAX.) ($V_{GS} = -10 \text{ V}$, $I_D = -2.5 \text{ A}$)
 $R_{DS(on)2} = 160 \text{ m}\Omega$ (MAX.) ($V_{GS} = -4 \text{ V}$, $I_D = -2.0 \text{ A}$)
- Low C_{iss} : $C_{iss} = 840 \text{ pF}$ (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1710AG	Power SOP8

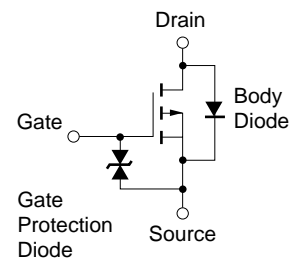
PACKAGE DRAWING (Unit : mm)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±5.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	±20	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

EQUIVALENT CIRCUIT



Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$

2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 1.1 \text{ mm}$

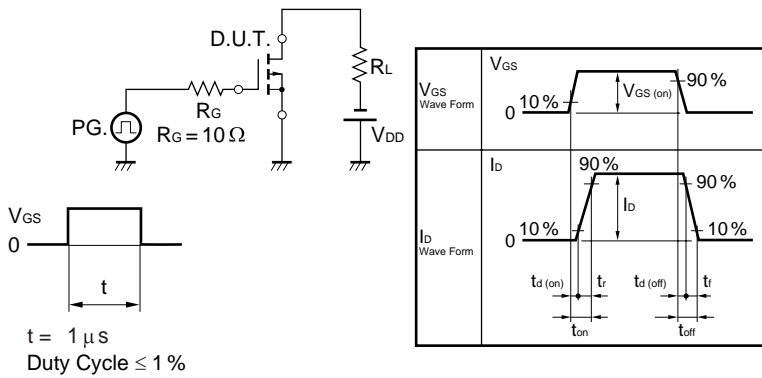
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

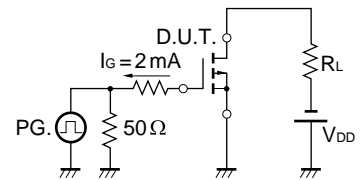
ELECTRICAL CHARACTERISTICS (TA = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}, I_D = -2.5\text{ A}$		45	70	mΩ
	$R_{DS(on)2}$	$V_{GS} = -4\text{ V}, I_D = -2.0\text{ A}$		91	160	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-1.0	-1.8	-2.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -2.5\text{ A}$	3.0	5.6		S
Drain Leakage Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-10	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			±10	μA
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}$		840		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$		570		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		190		pF
Turn-on Delay Time	$t_{d(on)}$	$I_D = -2.5\text{ A}$		13		ns
Rise Time	t_r	$V_{GS(on)} = -10\text{ V}$		66		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{DD} = -15\text{ V}$		82		ns
Fall Time	t_f	$R_G = 10\ \Omega$		52		ns
Total Gate Charge	Q_G	$I_D = -5.0\text{ A}$		27.3		nC
Gate to Source Charge	Q_{GS}	$V_{DD} = -24\text{ V}$		2.7		nC
Gate to Drain Charge	Q_{GD}	$V_{GS} = -10\text{ V}$		8.2		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 5.0\text{ A}, V_{GS} = 0\text{ V}$		0.81		V
Reverse Recovery Time	t_{rr}	$I_F = 5.0\text{ A}, V_{GS} = 0\text{ V}$		61		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 50\text{ A}/\mu\text{s}$		71		nC

TEST CIRCUIT 1 SWITCHING TIME

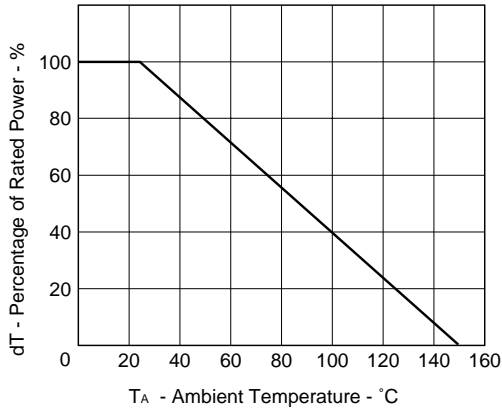


TEST CIRCUIT 2 GATE CHARGE

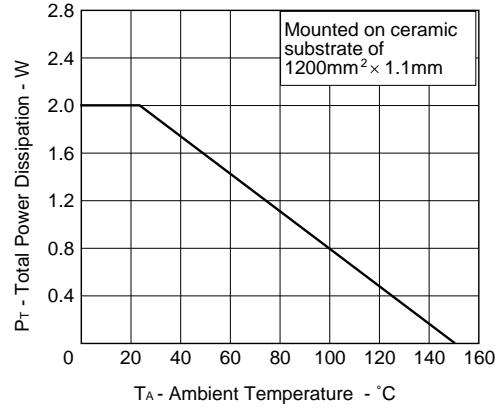


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

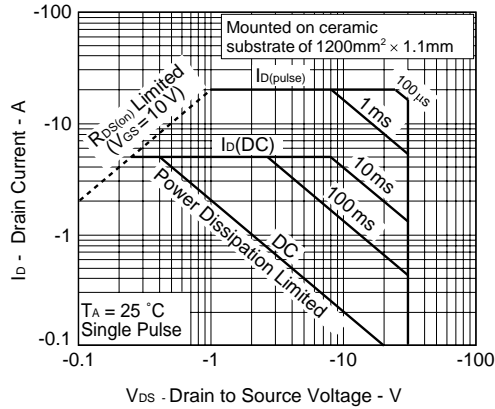
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



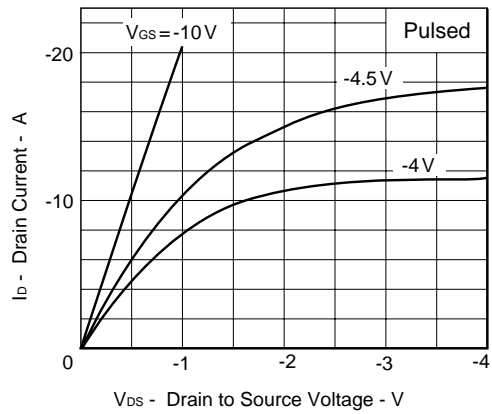
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



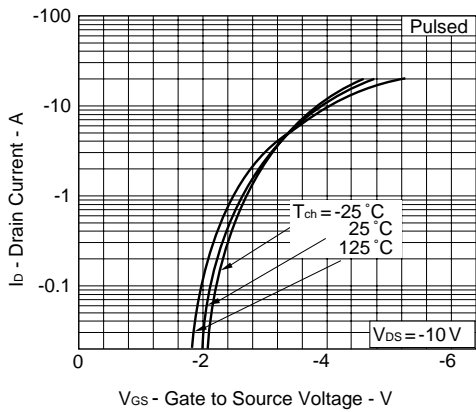
FORWARD BIAS SAFE OPERATING AREA



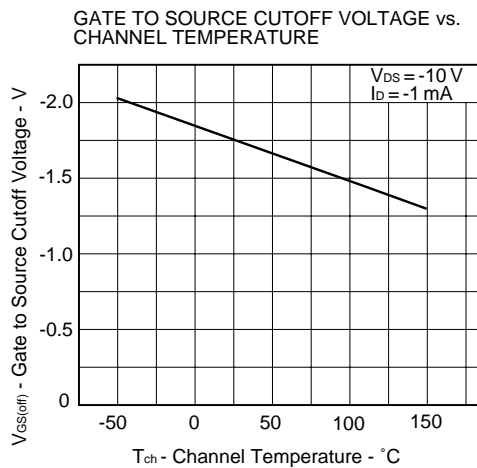
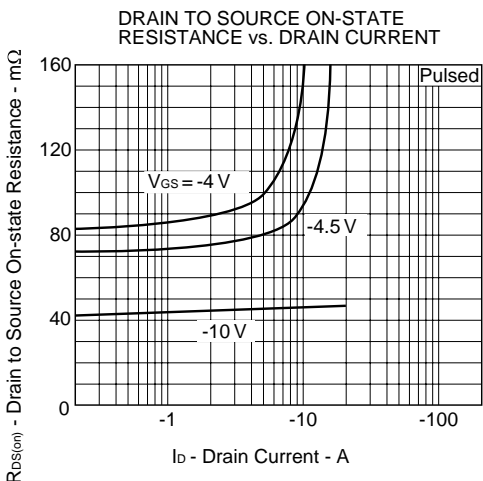
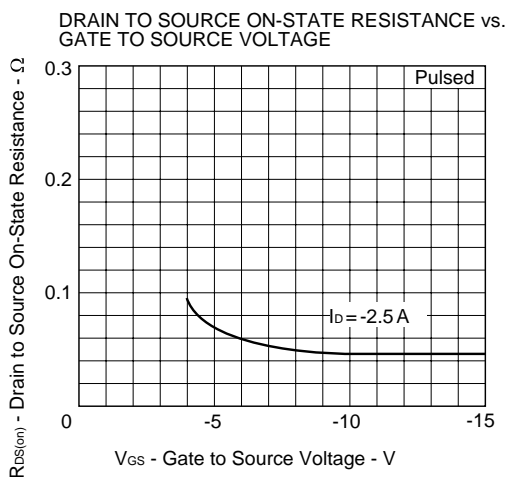
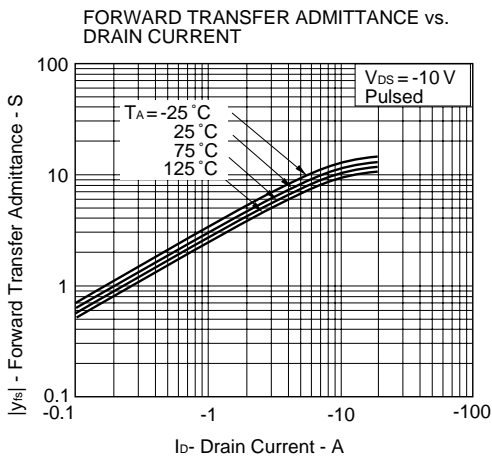
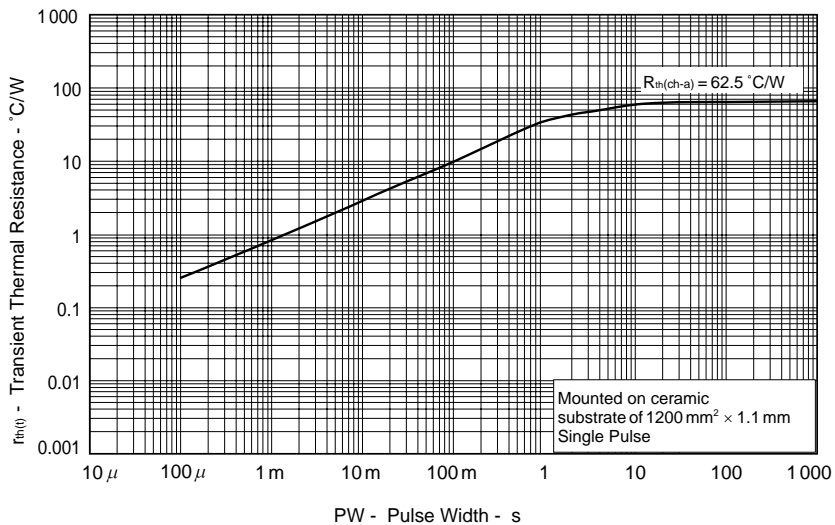
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

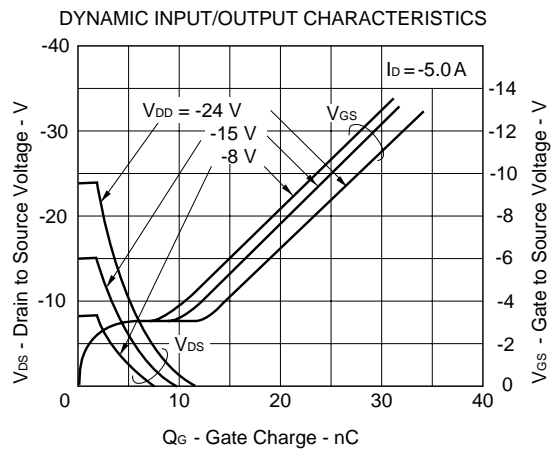
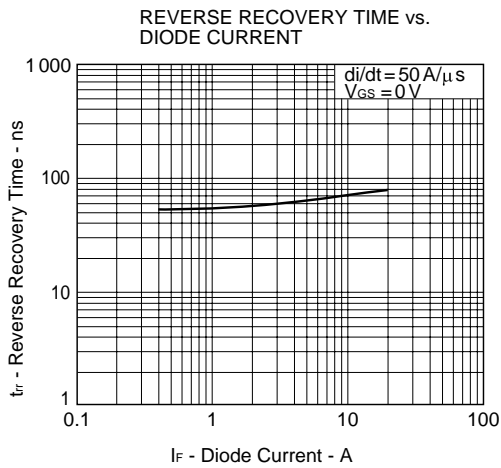
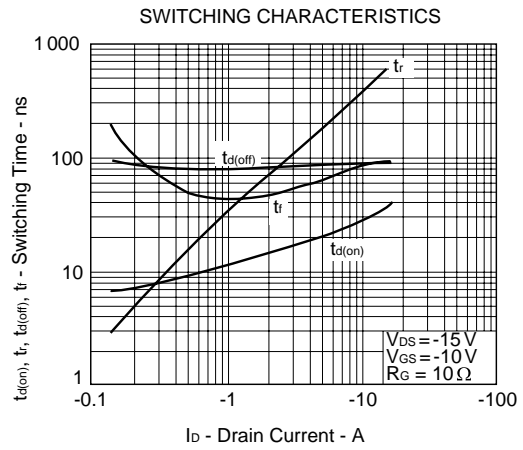
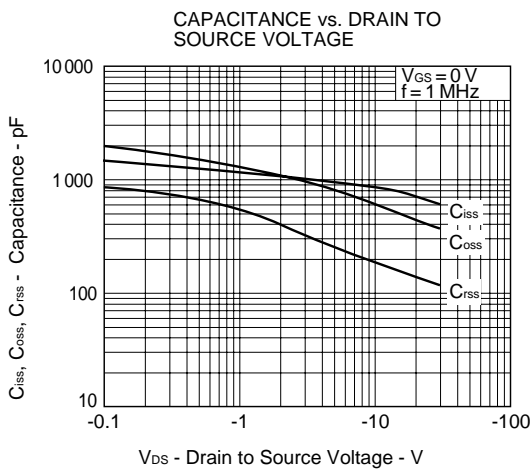
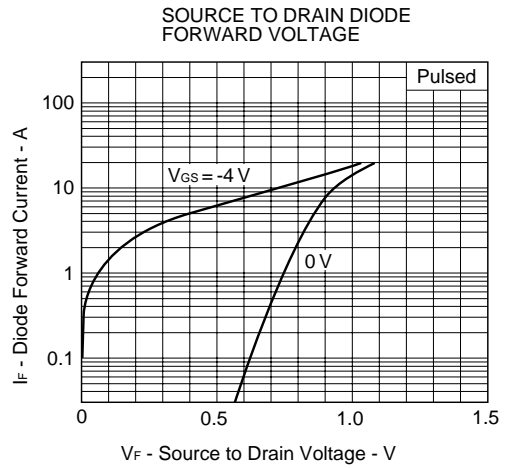
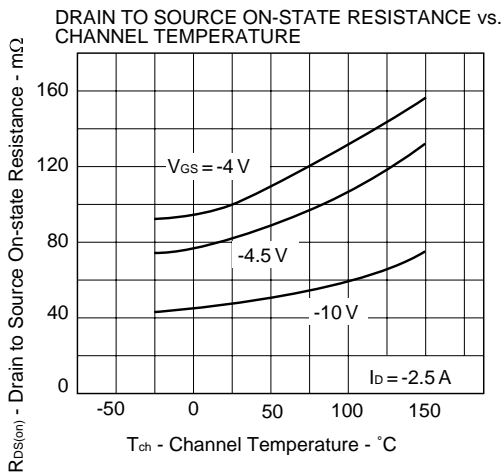


FORWARD TRANSFER CHARACTERISTICS



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





[MEMO]

[MEMO]

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Anti-radioactive design is not implemented in this product.