NEC

BiCMOS INTEGRATED CIRCUIT

μPC1935

DC-DC CONVERTER CONTROLLER IC

DESCRIPTION

The μPC1935 is a low-voltage input DC-DC converter controller IC that can configure a three-output (stepup × 2, inverted output × 1) DC-DC converter at an input voltage of 3, 3.3, or 5 V.

Because of its wide operating voltage range, this IC can also be used to control DC-DC converters using an AC adapter for input.

FEATURES

- Low supply voltage: 2.5 V
- Operating voltage range: 2.5 to 20 V (breakdown voltage: 30 V)
- Can control three output channels.
- Timer latch circuit for short circuit protection
- Ceramic capacitor with a low capacitance (0.1 μF) can be used for short circuit protection.
- Dead times of channels 2 (stepup) and 3 (inverted output) can be set from external resistors. Dead time of channel 1 (stepup) is internally fixed to 85 %.
- Soft start of each channel can be set independently.
- Each channel can be turned ON/OFF independently.

ORDERING INFORMATION

Part Number	Package
μPC1935GR	16-pin plastic TSSOP (225 mil)

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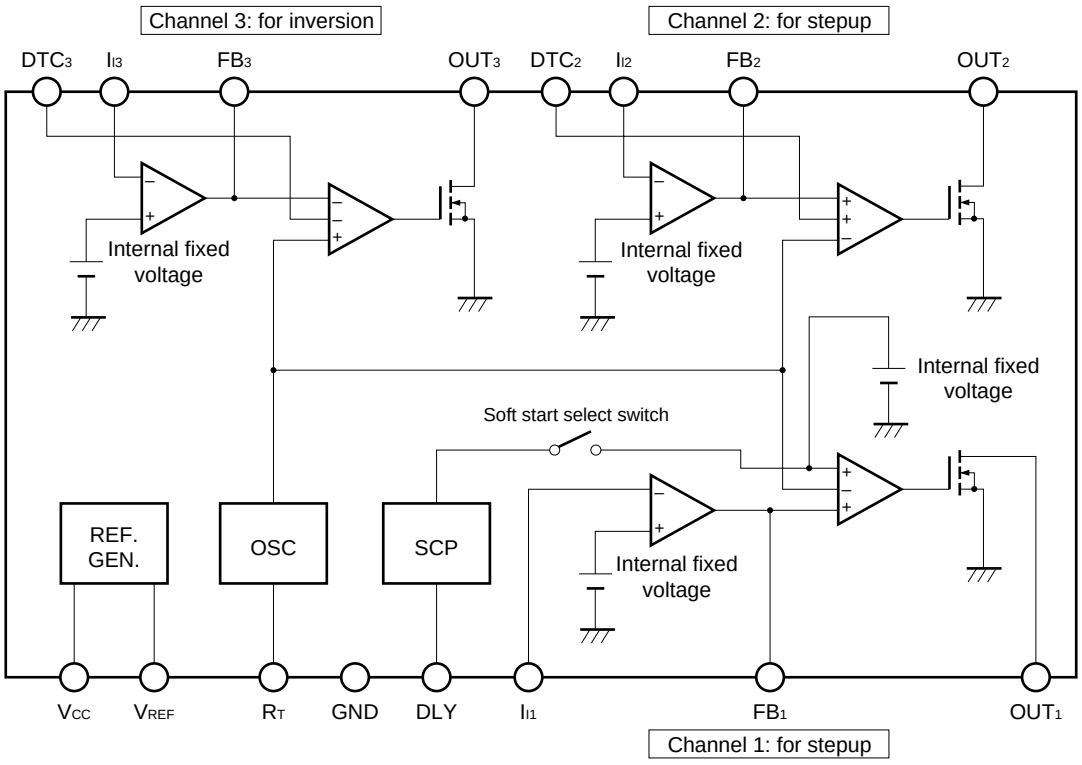
Date Published December 1998 N CP(K)
Printed in Japan

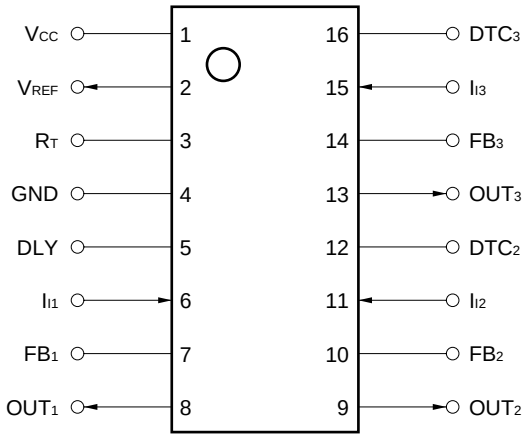
The mark ★ shows major revised points.

BLOCK DIAGRAM



PIN CONFIGURATION

16-pin plastic TSSOP (225 mil)
μPC1935GR



PIN FUNCTIONS

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	V_{CC}	Power supply	9	OUT_2	Channel 2 open-drain output
2	V_{REF}	Reference voltage output	10	FB_2	Channel 2 error amplifier output
3	R_T	Frequency setting resistor connection	11	I_{I2}	Channel 2 error amplifier inverted input
4	GND	Ground	12	DTC_2	Channel 2 dead time setting
5	DLY	Short-circuit protection/channel 1 soft start capacitor connection	13	OUT_3	Channel 3 open-drain output
6	I_{I1}	Channel 1 error amplifier inverted input	14	FB_3	Channel 3 error amplifier output
7	FB_1	Channel 1 error amplifier output	15	I_{I3}	Channel 3 error amplifier inverted input
8	OUT_1	Channel 1 open-drain output	16	DTC_3	Channel 3 dead time setting

1. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (Unless otherwise specified, T_A = 25 °C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	30	V
Output voltage	V_O	30	V
Output current (open-drain output)	I_D	21	mA
Total power dissipation	P_T	400	mW
Operating temperature	T_A	–20 to +85	°C
Storage temperature	T_{stg}	–55 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

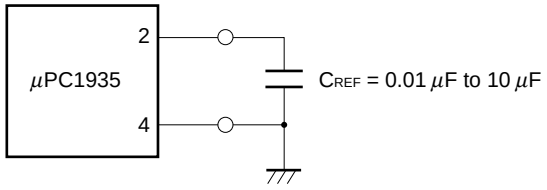
★ **Recommended Operating Conditions**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	2.5		20	V
Output voltage	V_O	0		20	V
Output current	I_O			20	mA
Operating temperature	T_A	–20		+85	°C
Oscillation frequency	f_{OSC}	20		800	kHz

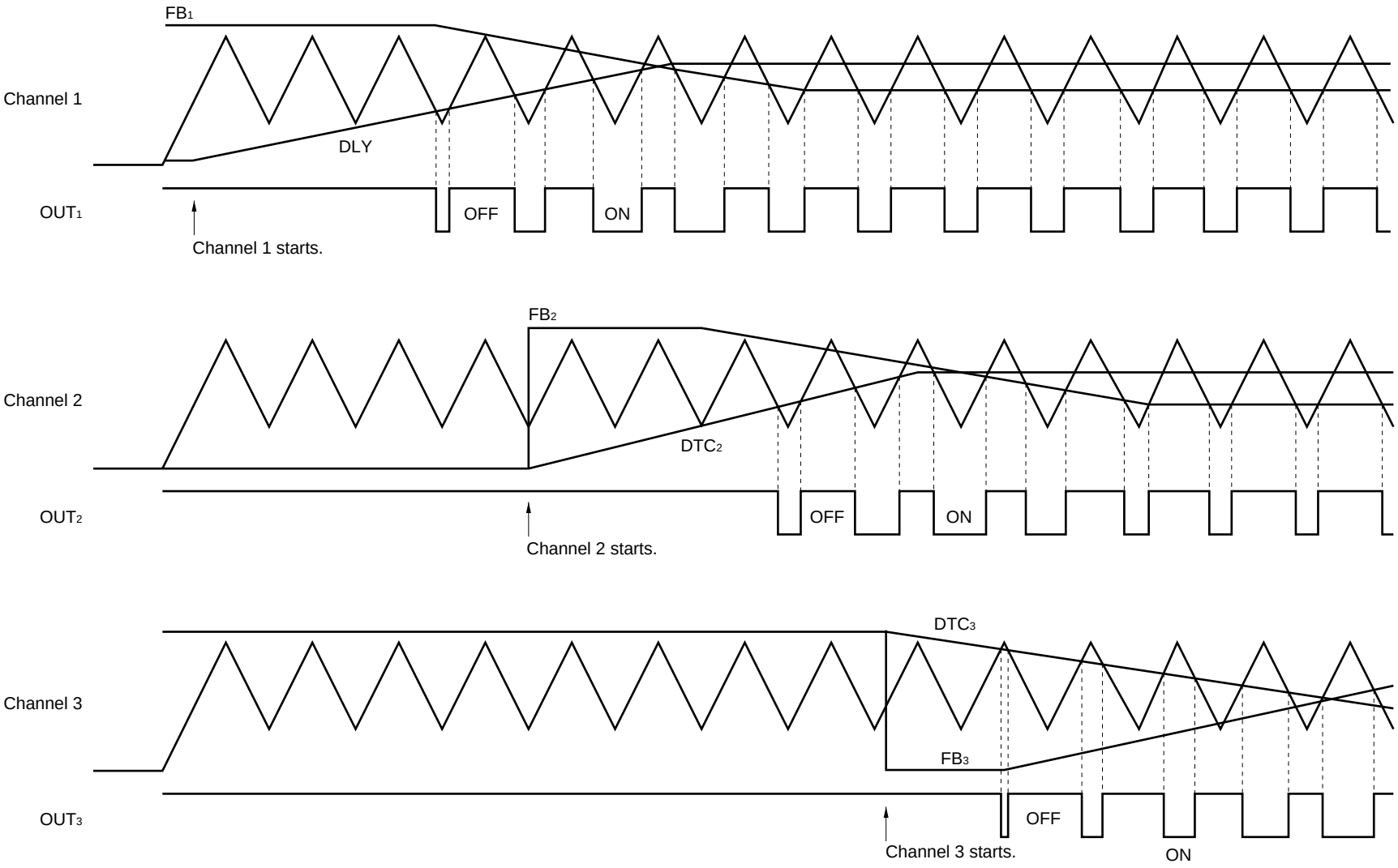
★ **Electrical Specifications (Unless otherwise specified, T_A = 25 °C, V_{CC} = 3 V, f_{OSC} = 100 kHz)**

Block	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Under voltage lock-out section	Start-up voltage	$V_{CC\ (L\text{-}H)}$	I_{REF} = 0.1 mA		1.57		V
	Operation stop voltage	$V_{CC\ (H\text{-}L)}$	I_{REF} = 0.1 mA		1.5		V
	Hysteresis voltage	V_H	I_{REF} = 0.1 mA	30	70		mV
	Reset voltage (timer latch)	V_{CCR}	I_{REF} = 0.1 mA		1.0		V
Reference voltage section	Reference voltage	V_{REF}	I_{REF} = 1 mA	2.0	2.1	2.2	V
	Line regulation	REG_{IN}	2.5 V ≤ V_{CC} ≤ 20 V		2	12.5	mV
	Load regulation	REG_L	0.1 mA ≤ I_{REF} ≤ 1 mA		1	7.5	mV
	Temperature coefficient	$\Delta V_{REF}/\Delta T$	–20 °C ≤ T_A ≤ +85 °C, I_{REF} = 0 A		0.5		%
Oscillation section	f_{OSC} setting accuracy	Δf_{OSC}	R_T = 18 kΩ	–20		+30	%
	f_{OSC} total stability	Δf_{OSC}	–20 °C ≤ T_A ≤ +85 °C, 2.5 V ≤ V_{CC} ≤ 20 V	–30		+50	%
Duty setting section	Input bias current	I_{BD}	(Channels 2 and 3 only)			1.0	μA
	Channel 1 maximum duty	$D_{MAX.}$			85		%
	Channel 1 soft start time	t_{SS}	C_{DLY} = 0.1 μF		50		ms
	Low-level threshold voltage	$V_{TH\ (L)}$	Duty = 0 % (channels 1 and 2) Duty = 100 % (channel 3)		1.2		V
	High-level threshold voltage	$V_{TH\ (H)}$	Duty = 100 % (channel 2) Duty = 0 % (channel 3)		1.6		V
Error amplifier section	Input threshold voltage	V_{ITH}		0.285	0.3	0.315	V
	Input bias current	I_B		–100		100	nA
	Open loop gain	A_V	V_O = 0.3 V	70	80		dB
	Unity gain	f_{unity}	V_O = 0.3 V		1.5		MHz
	Maximum output voltage (+)	V_{OM^+}	I_O = –45 μA	1.6			V
	Maximum output voltage (–)	V_{OM^-}	I_O = 45 μA			0.5	V
	Maximum sink current	I_{Osink}	V_{FB} = 0.5 V	0.8	1.4		mA
	Output source current	$I_{Osource}$	V_{FB} = 1.6 V		–70	–45	μA
Output section	Output ON voltage	V_{OL}	R_L = 150 Ω			0.6	V
	Rise time	t_r	R_L = 150 Ω		50		ns
	Fall time	t_f	R_L = 150 Ω		50		ns
Short-circuit protection section	Input sense voltage	V_{TH1}, V_{TH2}	Channels 1 and 2		1.9		V
		V_{TH3}	Channel 3		0.63		V
	UV sense voltage	V_{UV}			0.8		V
	Source current on short-circuiting	I_{OUV}		1.0	1.6	2.7	μA
	Delay time	t_{DLY}	C_{DLY} = 0.1 μF		50		ms
Overall	Circuit operation current	I_{CC}	V_{CC} = 3 V		3.1		mA

★ **Caution Connect a capacitor of 0.01 μF to 10 μF to the V_{REF} pin.**

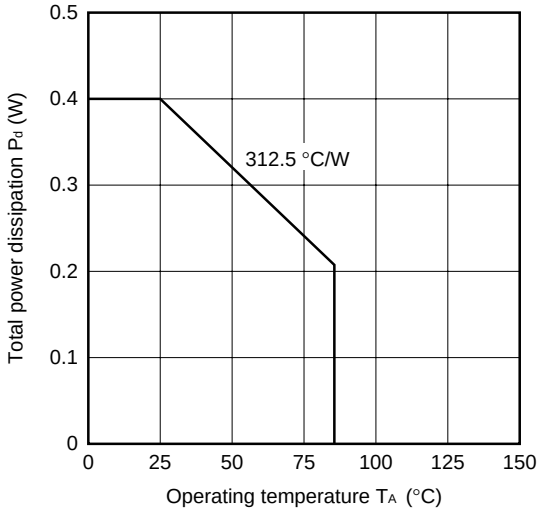


TIMING CHARTS (sequence operation of power application → channel 1 → channel 2 → channel 3)

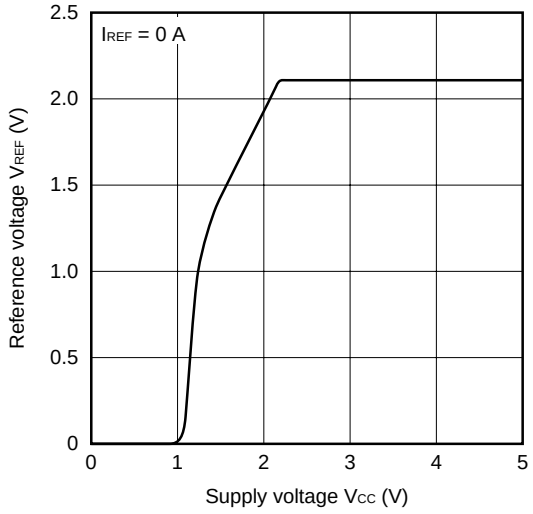


TYPICAL CHARACTERISTIC CURVES (Unless otherwise specified, V_{CC} = 3 V, f_{OSC} = 100 kHz, T_A = 25 °C)

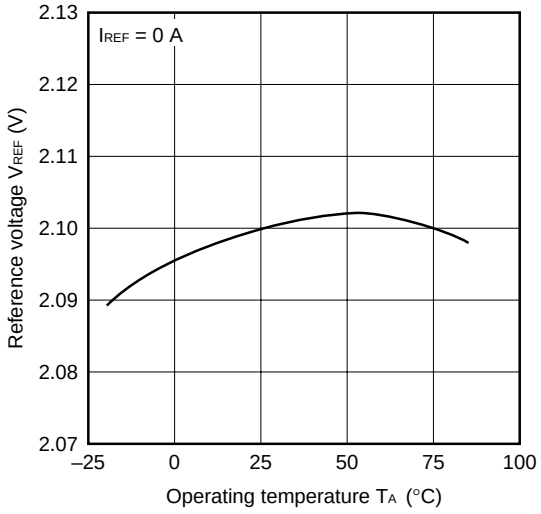
P_d –T_A



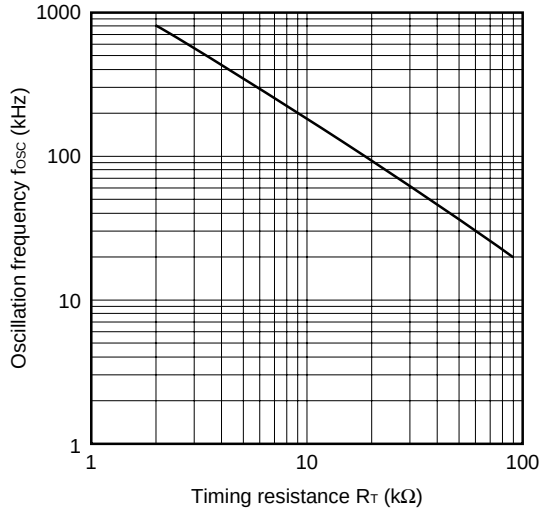
V_{REF} –V_{CC}



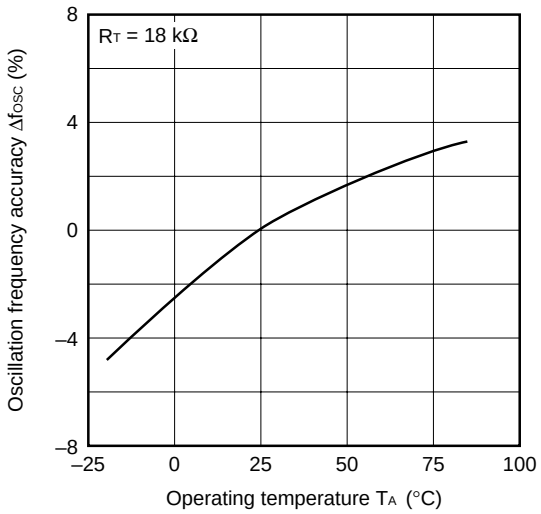
V_{REF} –T_A



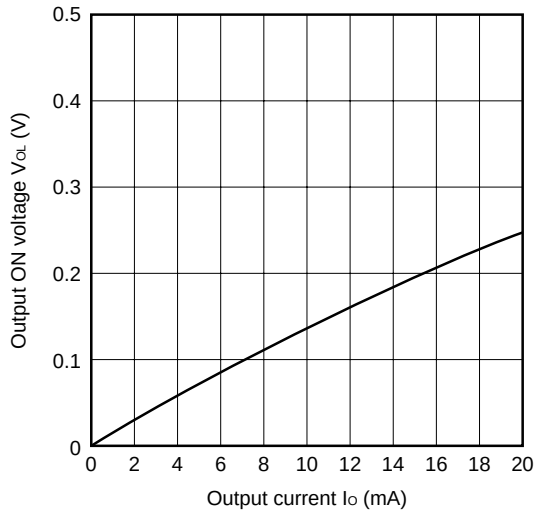
f_{OSC} –R_T



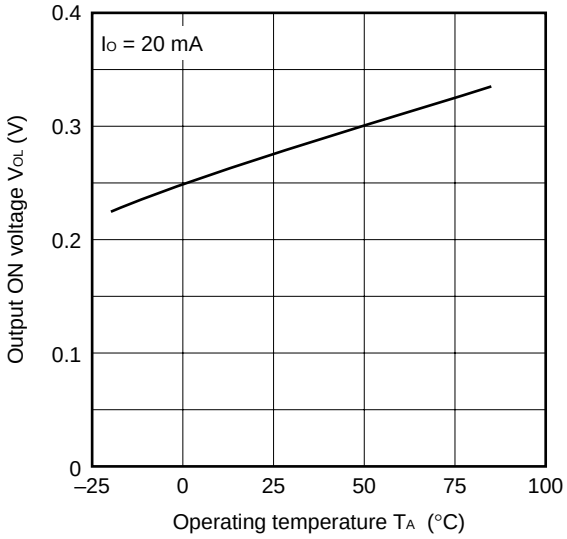
Δf_{OSC} –T_A



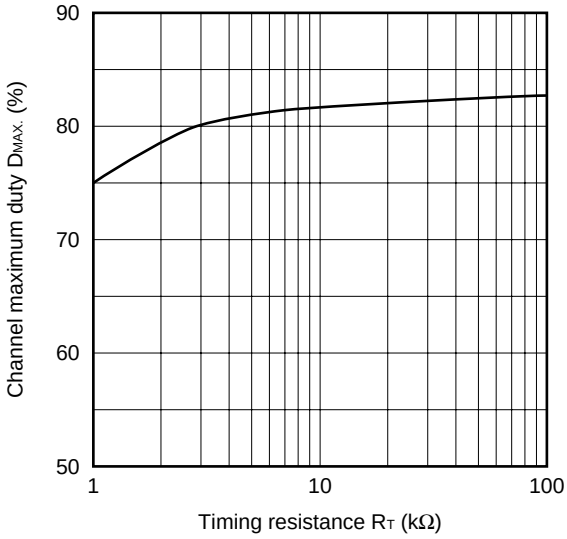
V_{OL} –I_O



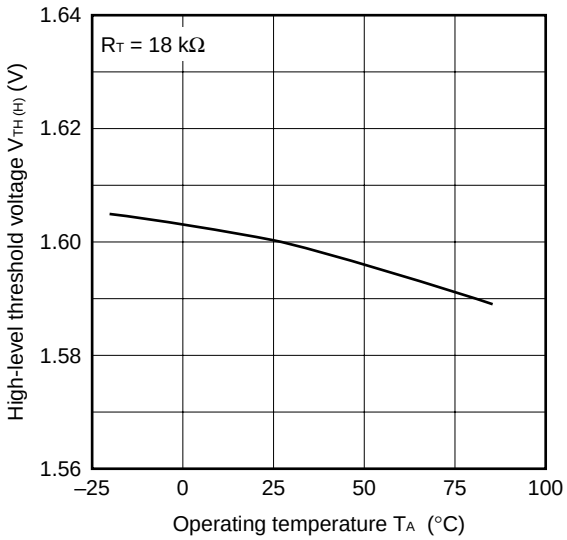
V_{OL} –T_A



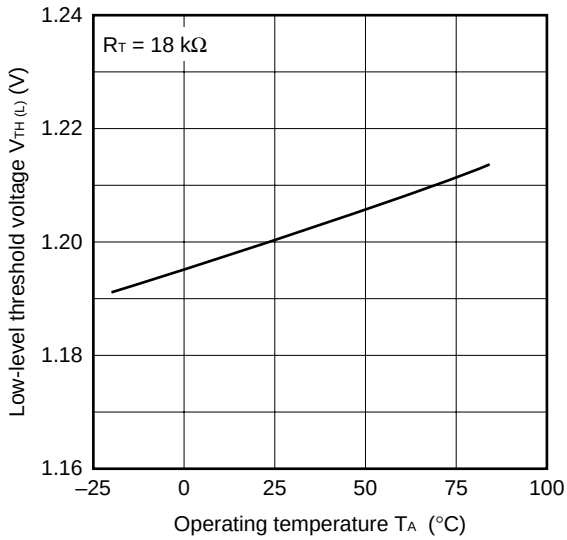
$D_{MAX.}$ –R_T



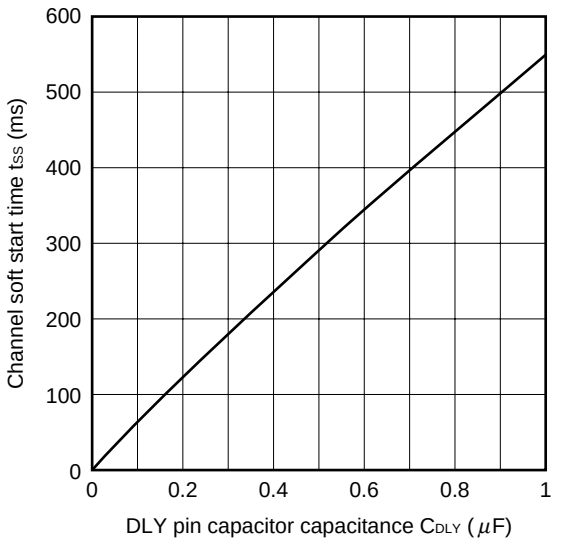
$V_{TH\ (H)}$ –T_A



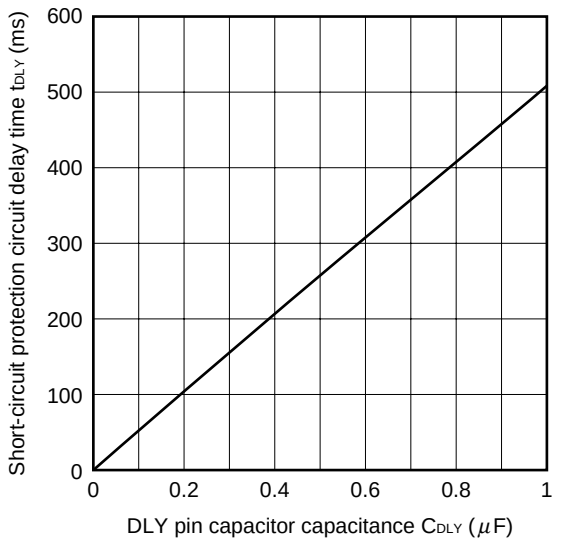
$V_{TH\ (L)}$ –T_A



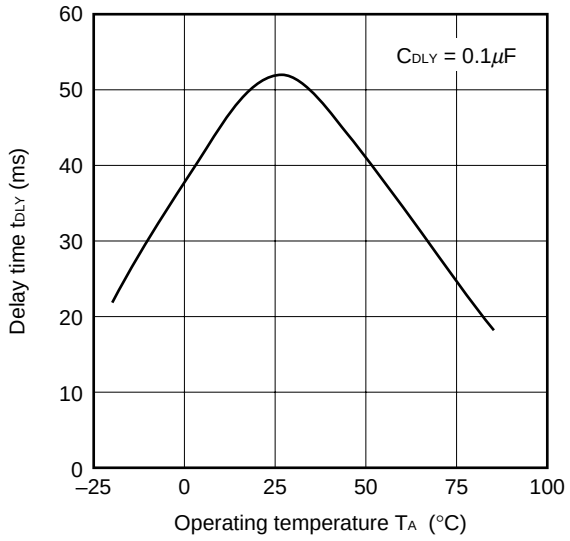
t_{SS}–C_{DLY}



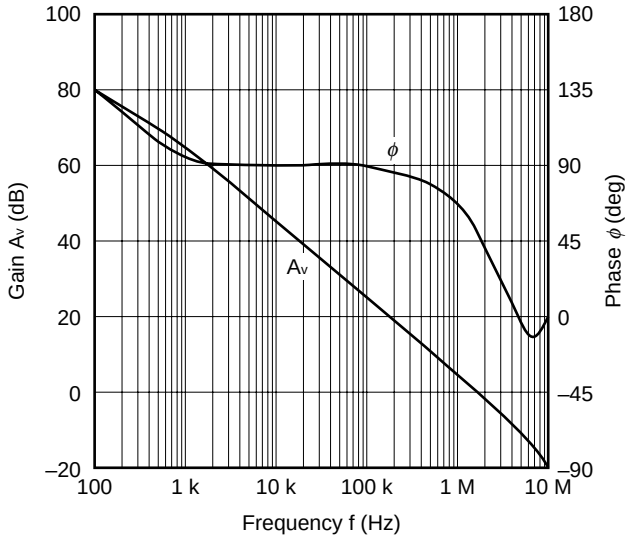
t_{DLY}–C_{DLY}



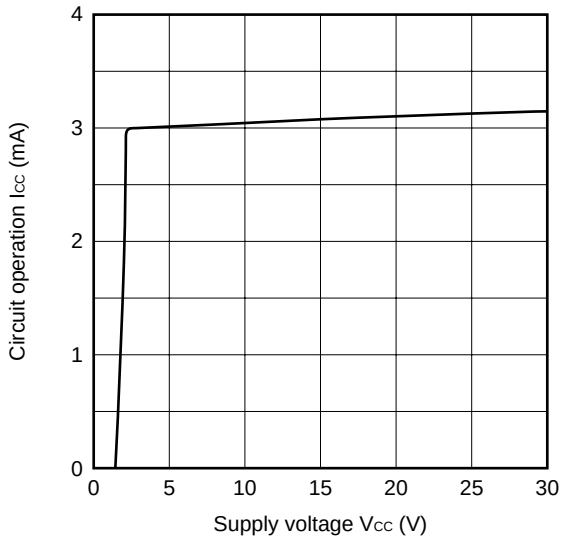
t_{DLY}–T_A



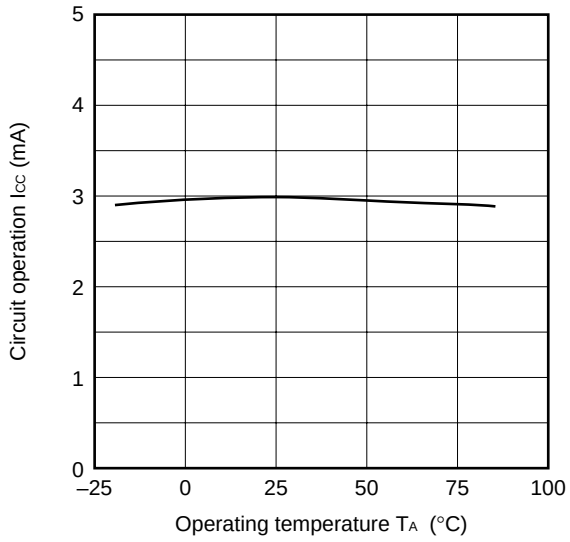
A_V, ϕ–f



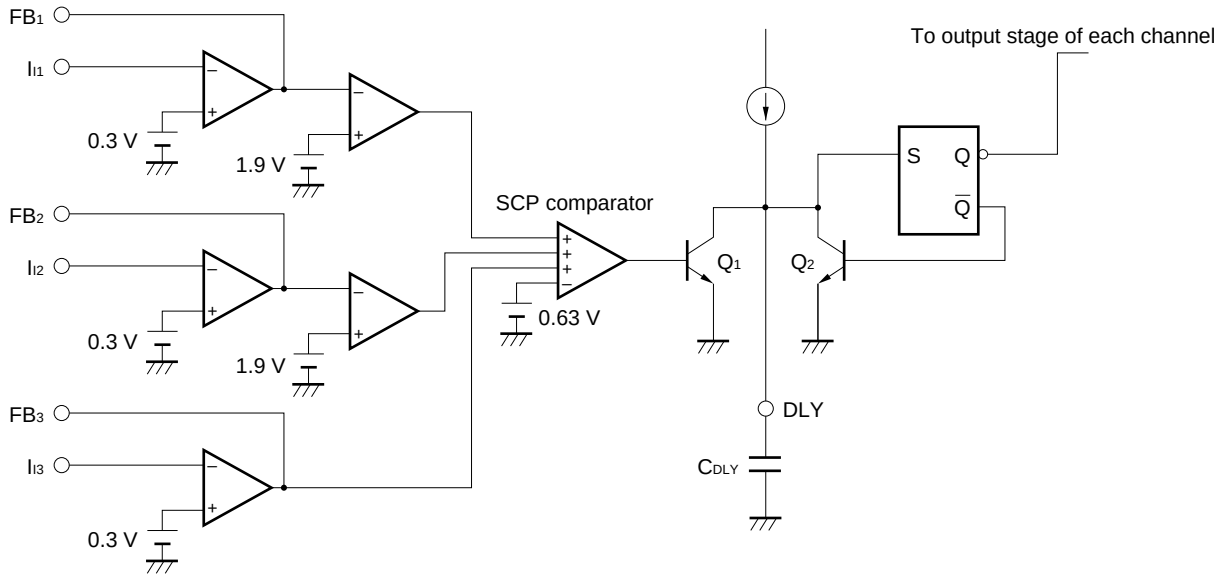
I_{CC}–V_{CC}



I_{CC}–T_A



2. TIMER LATCH CIRCUIT OPERATION FOR SHORT CIRCUIT PROTECTION (S.C.P.)



The timer latch circuit operates as follows:

If the converter output of each channel drops, the FB output of the error amplifier goes high (FB_3 output goes low), and the input level of the SCP comparator drops. If the input level of the SCP comparator drops below 0.63 V, the output of the comparator is inverted, and Q_1 turns OFF.

When Q_1 turns OFF, the constant-current supply charges C_{DLY} via the DLY pin. The DLY pin is internally connected to a flip-flop. When the DLY pin voltage reaches the UV detection voltage (V_{UV} = 0.8 V (TYP.)), the output Q of the flip-flop goes low, and the output stage of each channel is latched to OFF.

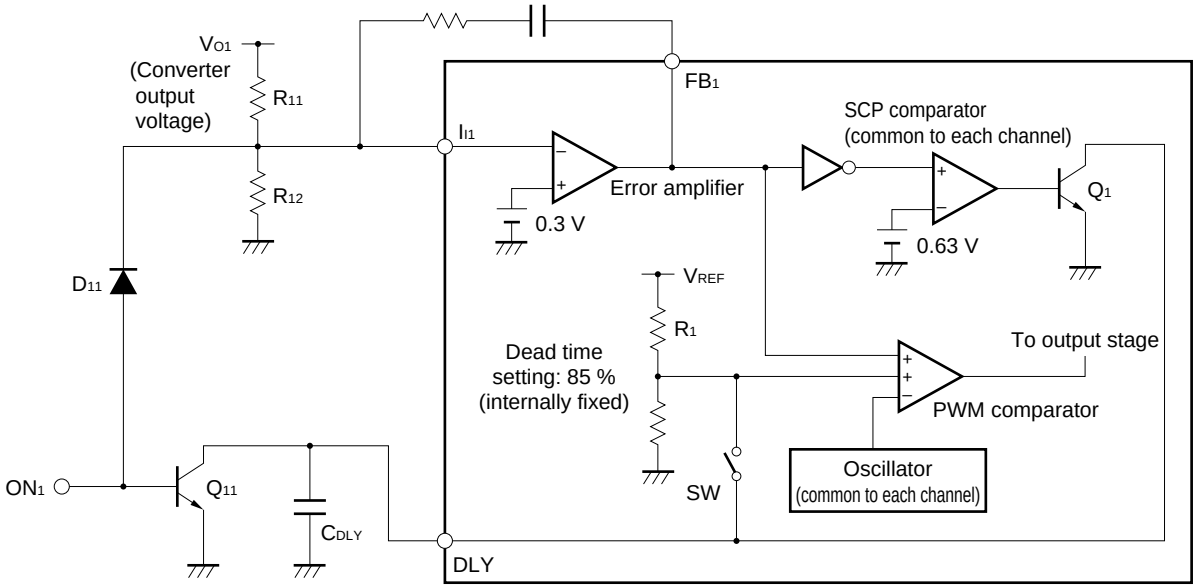
The logic of channels 1 and 2 is reverse to that of channel 3. Consequently, an inverter circuit is inserted between the FB output of channels 1 and 2, and SCP comparator input.

The input detection voltage (V_{TH}) of the timer latch is 1.9 V (TYP.) for channels 1 and 2, and 0.63 V (TYP.) for channel 3.

3. ON/OFF CONTROL

The diagram below is an example of a circuit that turns each channel ON/OFF independently. In this example, the action of turning each channel ON/OFF is controlled by negative logic ($\overline{ON}$/OFF).

3.1 Channel 1 (for stepup)



The sequence in which channel 1 is turned ON/OFF is as follows:

The signal that turns channel 1 ON/OFF is input from ON_1. For channel 1, soft start or timer latch (SCP) is internally selected. Soft start is executed when the first start signal is input. When the end of soft start is detected, the soft start select switch is turned OFF and the timer latch circuit operates.

(1) When ON_1 is high: OFF status

Q_{11}: ON → DLY pin: Low level → Output duty of PWM comparator: 0 %

D_{11}: ON → I_{I1} pin: High level → FB_1 output: Low level

(2) When ON_1 is low: ON status (start up)

Q_{11}: OFF → C_{DLY} is charged in the sequence of [V_{REF} → R_1 → SW → DLY pin → C_{DLY}] → Soft start

D_{11}: OFF → I_{I1} pin: Low level → FB_1 output: High level

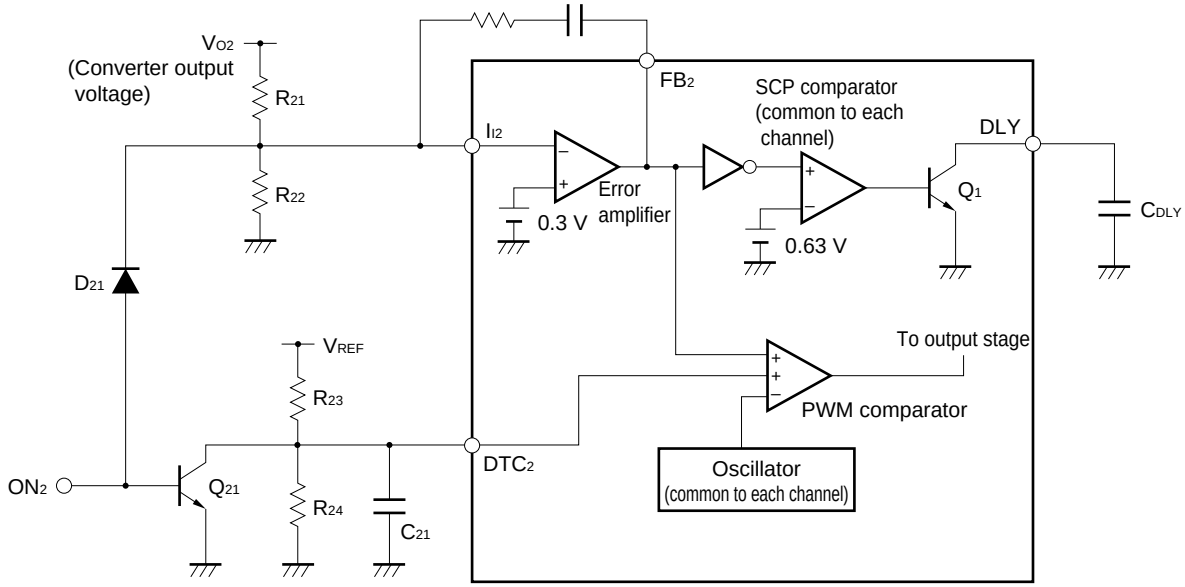
(3) When ON_1 goes high again after start up (SW: OFF): OFF status

Q_{11}: ON → DLY pin: Low level (Nothing happens because SW is OFF.)

D_{11}: ON → I_{I1} pin: High level → FB_1 output: Low level → PWM comparator output duty: 0 %
→ Converter output voltage (V_{O1}) drops.

★ **Remark** Even if start up is executed by making ON_1 low again after (3), soft start is not executed because the soft start select switch (SW) remains OFF. To execute soft start of channel 1 again, drop V_{CC} to 0 V once.

3.2 Channel 2 (for stepup)



The sequence in which channel 2 is turned ON/OFF is as follows:

The signal that turns channel 2 ON/OFF is input from ON_2. The PWM converter can be turned ON/OFF by controlling the level of the DTC_2 pin. However, it is necessary to keep the level of the FB_2 output low (the SCP comparator input high) so that the timer latch does not start when the PWM converter is OFF. In this circuit example, the FB_2 output level is controlled by controlling the level of the I_{I2} pin.

(1) When ON_2 is high: OFF status

Q_{21}: ON → DTC_2 pin: Low level → Output duty of PWM comparator: 0 %

D_{21}: ON → I_{I2} pin: High level → FB_2 output: Low level → SCP comparator output: High level → Timer latch stops.

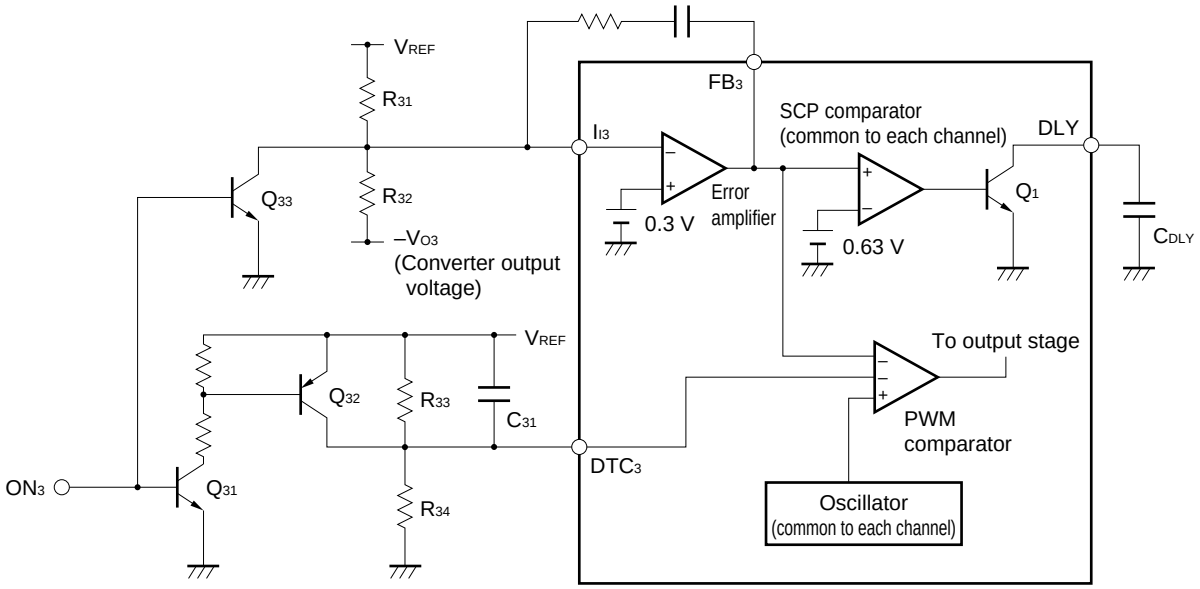
(2) When ON_2 is low: ON status

Q_{21}: OFF → C_{21} is charged in the sequence of [V_{REF} → R_{23} → C_{21}] → DTC_2 pin voltage rises → Soft start

D_{21}: OFF → I_{I2} pin: Low level → FB_2 output: High level → SCP comparator output: Low level → Q_1 is OFF → Charging C_{DLY} starts (timer latch start).

Caution Keep the low-level voltage of the DTC_2 pin within 1.2 V and the high-level voltage of the I_{I2} pin at 0.3 V or higher. The maximum voltage that is applied to the I_{I2} pin must be equal to or lower than V_{REF}.

3.3 Channel 3 (for inverted output)



The sequence in which channel 3 is turned ON/OFF is as follows:

The signal that turns channel 3 ON/OFF is input from ON_3. The PWM converter can be turned ON/OFF by controlling the level of the DTC_3 pin. However, it is necessary to keep the level of the FB_3 output high so that the timer latch does not start when the PWM converter is OFF. In this circuit example, the FB_3 output level is controlled by controlling the level of the I_{I3} pin.

Because channel 3 supports an inverted converter, its PWM comparator logic is different from that of channels 1 and 2.

(1) When ON_3 is high: OFF status

Q_{31}: ON → Q_{32}: ON → DTC_3 pin: High level → Output duty of PWM comparator: 0 %

Q_{33}: ON → I_{I3} pin: Low level → FB_3 output: High level → SCP comparator output: High level → Q_1 is ON.
→ Timer latch stops.

(2) When ON_3 is low: ON status

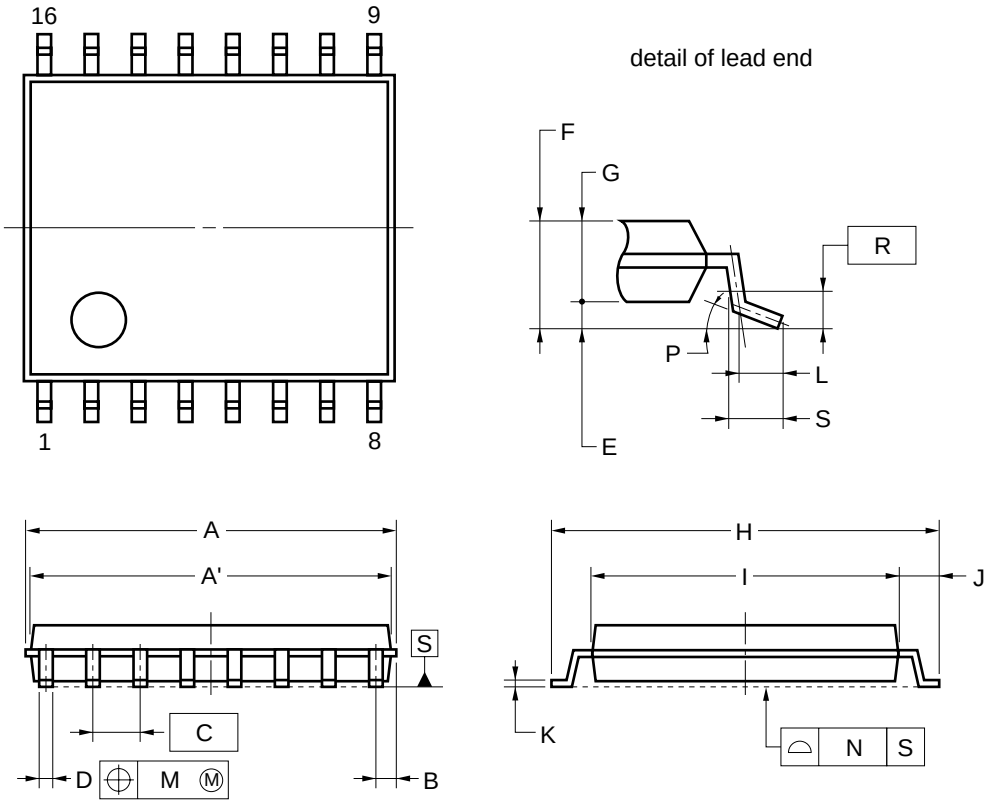
Q_{31}: OFF → Q_{32} is OFF. → C_{31} is charged in the sequence of [V_{REF} → C_{31} → R_{34}] → DTC_3 pin voltage drops.
→ Soft start

Q_{33}: OFF → I_{I3} pin: High level → FB_3 output: Low level → SCP comparator output: Low level → Q_1: OFF
→ Charging C_{DLY} starts (timer latch start).

Caution Keep the high-level voltage of the DTC_3 pin at 1.6 V or higher and the low-level voltage of the I_{I3} pin within 0.3 V. The maximum voltage that is applied to the I_{I3} pin must be equal to or lower than V_{REF}.

4. PACKAGE DRAWING

16 PIN PLASTIC TSSOP (225 mil)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.15±0.15
A'	5.0±0.1
B	0.375 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.06}_{-0.04}$
E	$0.09^{+0.06}_{-0.04}$
F	$1.01^{+0.09}_{-0.06}$
G	0.92
H	6.4±0.2
I	4.4±0.1
J	1.0±0.2
K	$0.145^{+0.055}_{-0.045}$
L	0.5
M	0.10
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.6±0.15

S16GR-65-PJG

★ 5. RECOMMENDED SOLDERING CONDITIONS

Recommended solder conditions for this product are described below.

For details on recommended soldering conditions, refer to Information Document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Surface mount type

μPC1935GR: 16-pin plastic TSSOP (225 mil)

Soldering Method	Soldering Conditions	Symbol of Recommended Conditions
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX. (210 °C MIN.), Number of times: 3 MAX.	IR35-00-3
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX. (200 °C MIN.), Number of times: 3 MAX.	VP15-00-3
Wave soldering	Soldering bath temperature: 260 °C MAX., Time: 10 seconds MAX., Number of times: 1, Preheating temperature: 120 °C MAX. (package surface temperature)	WS60-00-1

Caution Do not use two or more soldering methods in combination.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

M4 96.5