DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUITS

μPC8190K,μPC8191K

RX/TX-IF SiMMIC FOR W-CDMA

DESCRIPTION

The μPC8190K and μPC8191K are silicon monolithic integrated circuit designed as receiver (RX) and transmitter (TX) IF section for W-CDMA. The μPC8190K is a RX-IF IC including IF-AGC amplifier and demodulator. The μPC8191K is a TX-IF IC including IF-AGC amplifier and quadrature modulator. These two ICs are suitable for kit-use for W-CDMA IF section.

The ICs are developed using NEC's new ultra high speed silicon bipolar process.

FEATURES

- RX-IF: 380 MHz, TX-IF: 570 MHz
- Low power consumption
- Built-in power saving function
- Small size: 20-pin plastic QFN package (3.2 × 4.2 × 0.8 mm)

APPLICAION

- W-CDMA

ORDERING INFORMATION

Part Number	Package	Supplying Form
μPC8190K-E1	20-pin plastic QFN	• Embossed tape 12 mm wide.
μPC8191K-E1	(3.2 × 4.2 × 0.8 mm)	• Pin 1 indicates pull-out direction of tape
		• Qty 2.5 kpcs/reel

Remark To order evaluation samples, please contact your local NEC sales office.
Part number for sample order: μPC8190K, μPC8191K

Caution electro-static sensitive devices.

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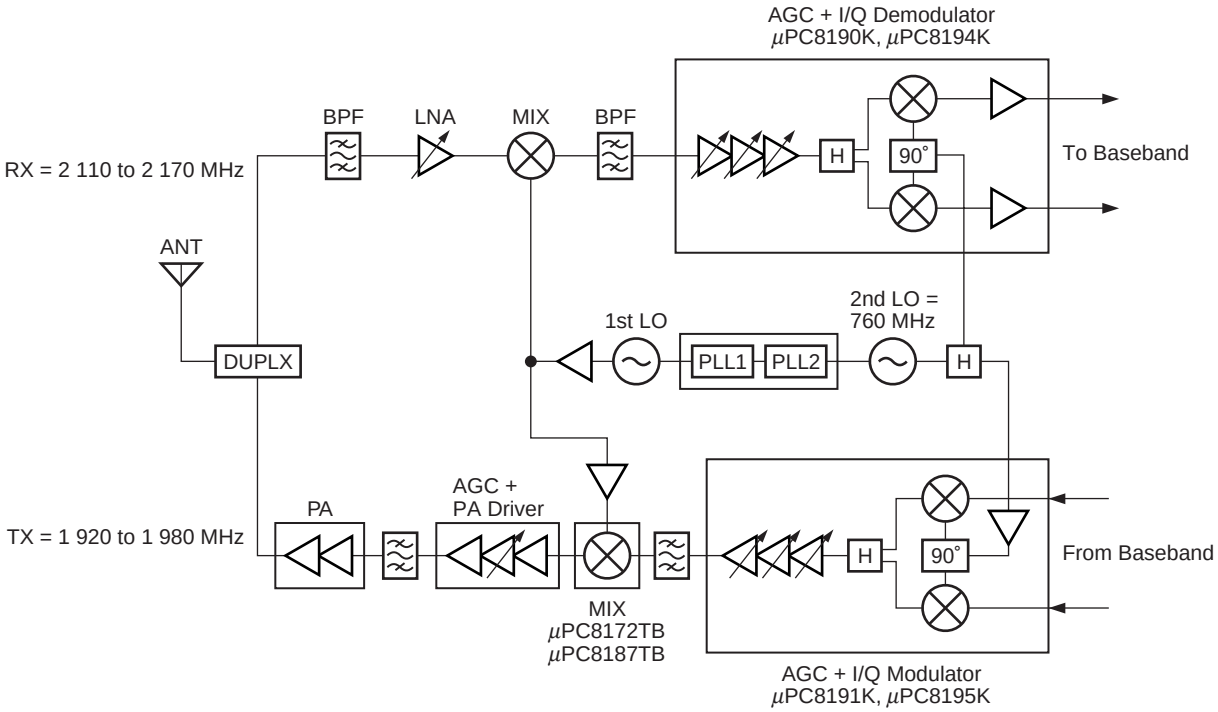
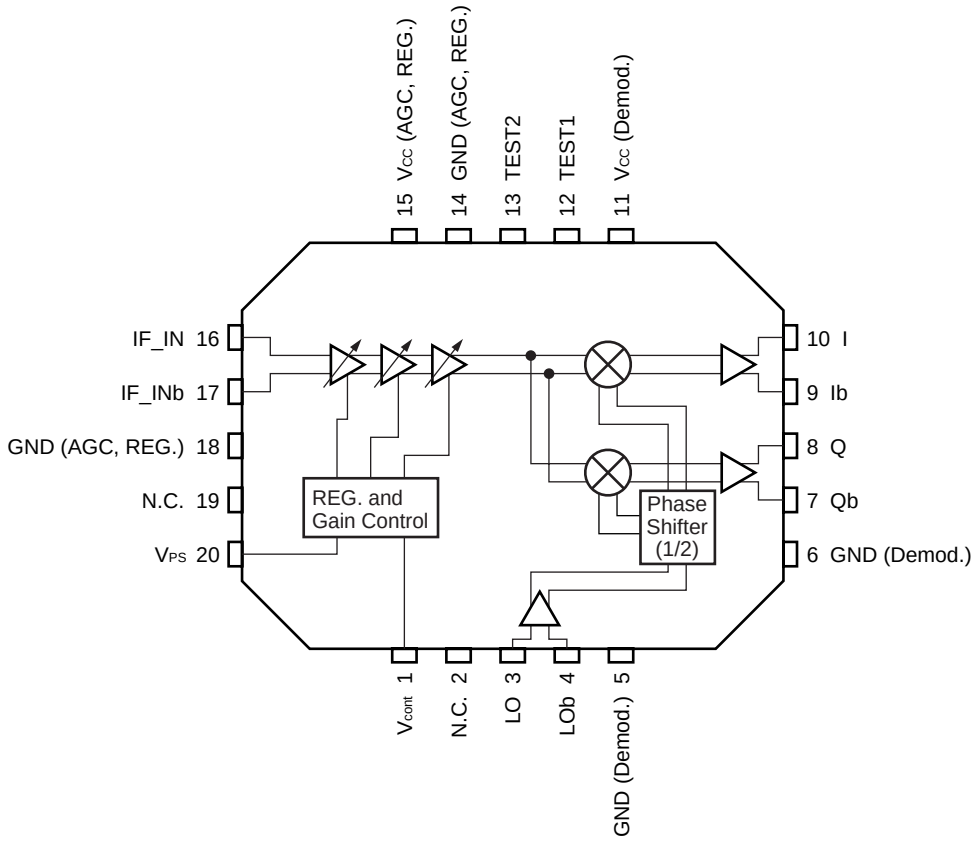
APPLICATION EXAMPLE

Variation of IF plan μPC8190K, μPC8191K: RX-IF = 380 MHz, TX-IF = 570 MHz
μPC8194K, μPC8195K: RX-IF = 190 MHz, TX-IF = 380 MHz

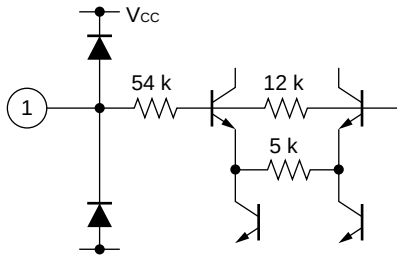
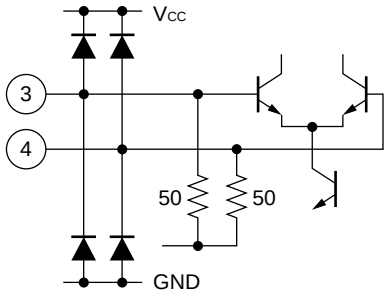
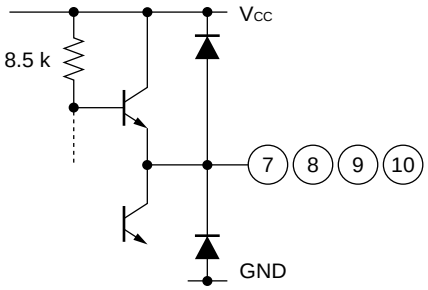


INTERNAL BLOCK DIAGRAM AND PIN CONFIGURATION – μPC8190K (RX) –

(Top View)

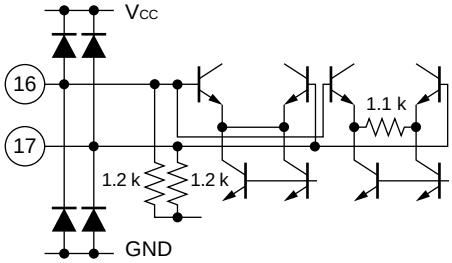
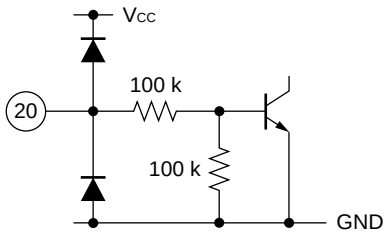


PIN EXPLANATIONS – μPC8190K (RX) –

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (TYP.) (V) Note	Functions and Applications	Internal Equivalent Circuits
1	V_{cont}	0 to 3.0	–	Gain cnotrol pin of AGC amplifier. Variable gains are available in accordance with applied voltage.	
2 19	N.C.	–	–	Non connection. This pin is not connected to internal circuit. This pin should be opened or grounded.	———
3	LO	–	–	Local signal input pin of I/Q demodulator. Input frequency is 760 MHz.	
4	LOb	–	–	Bypass pin of local signal input for I/Q demodulator. In the case of single local input, this pin must be decoupled with capacitor ex. 100 to 1 000 pF.	
5 6	GND (Demod.)	0	–	Ground pin of I/Q demodulator. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impeadance.	———
7	Qb	–	–	I/Q/Ib/Qb signal output pins. Each pin is an emitter follower. Each of Ib and Qb is differential output of I and Q. Recommendable load impedance is 10 to 20 kΩ.	
8	Q	–	–		
9	Ib	–	–		
10	I	–	–		

Note Pin voltage is measured at V_{CC} = 3.0 V

– μPC8190K (RX) –

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (TYP.) (V) Note	Functions and Applications	Internal Equivalent Circuits
11	V_{CC} (Demod.)	2.7 to 3.3	–	Supply voltage pin of I/Q demodulator (phase shifter + I/Q Mixer).	———
12	TEST 1	0	–	TEST pin. In actual use, this pin should be grounded.	———
13	TEST 2	0	–		
14 18	GND (AGC, REG.)	0	–	Ground pin of AGC amplifier and internal regulator. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impedance.	———
15	V_{CC} (AGC, REG.)	2.7 to 3.3	–	Supply voltage pin of AGC amplifier and internal regulator.	———
16	IF_IN	–	–	IF signal input pin. This pin is input of AGC amplifier. Balance input between 16, 17 pin. Input frequency is 380 MHz.	
17	IF_INb	–	–	IF signal input pin. In the case of signal local input, this pin must be decoupled with capacitor.	
20	V_{PS}	H: 2.2 to V_{CC}	–	Power saving pin. This pin modulator can control Active/Sleep state with bias as follows. V_{PS} (V) / State: 0 to 0.5 – Sleep Mode 2.2 to 3 – Active Mode	
		L: 0 to 0.5			

Note Pin voltage is measured at V_{CC} = 3.0 V

ABSOLUTE MAXIMUM RATINGS – μPC8190K (RX) –

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	4.0	V
Applied Voltage	V_{PS}, V_{cont}	–0.3 to V_{CC} + 0.3	V
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	°C

RECOMMENDED OPERATING RANGE – μPC8190K (RX) –

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.3	V
Operating Ambient Temperature	T_A	–25	25	85	°C
IF Frequency	f_{IF}	–	380	–	MHz
Local Frequency	f_{LO}	–	760	–	MHz
Local Input Level	P_{LO}	–18	–15	–12	dBm

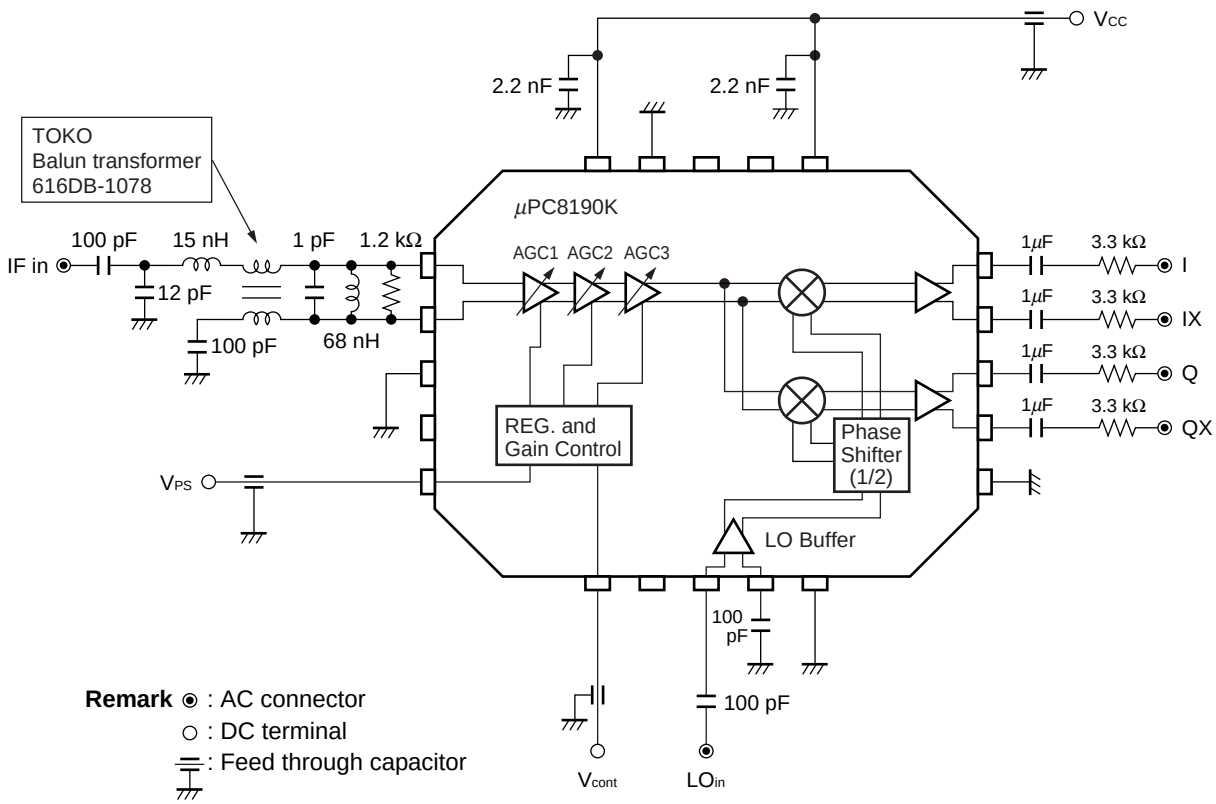
ELECTRICAL CHARACTERISTICS – μPC8190K (RX) – (Unless otherwise specified, V_{CC} = 3.0 V, T_A = +25°C, f_{IF} = 382.5 MHz, f_{LO} = 760 MHz, P_{LO} = –15 dBm, $f_{I/Q}$ = 2.5 MHz)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No input signal	–	9	12	mA
		At power-saving mode	–	–	1	μA
Voltage Gain	V_G1	V_{cont} = 2.5 V	68	77	–	dB
	V_G2	V_{cont} = 0.5 V	–	–20	–15	dB
Input 3rd Order Intercept Point	IIP_3	Gain = +65 dB (R_S= 600 Ω balanced), P_{IFin} = –70 dBm	–60	–55	–	dBm
		Gain = –10 dB (R_S= 600 Ω balanced), P_{IFin} = –10 dBm	0	3	–	dBm
Local Leakage	LOL	Leakage to I/Q port when local = 380 MHz and output = 30 mV_{P-P} balanced	–	–	–20	dBc
I/Q Bandwidth	$f_{I/Q}$	3 dB down	10	–	–	MHz
I/Q Maximum Output Swing	$V_{O\ (sat)}$	Balanced output	1	–	–	V_{P-P}
I/Q Gain Balance	AE	$f_{I/Q}$ = 2.5 MHz	–	–	Δ0.5	dB
I/Q Phase Error	PE	$f_{I/Q}$ = 2.5 MHz	–	–	±4	deg.
Gain Accuracy	Gacc	V_{cont} = 1 to 2 V	–	Δ4.6	Δ6	dB/V
Rise Time from Power-saving Mode	t_{PS}		–	–	20	μs
Rising Voltage from Power-saving Mode	$V_{PS\ on}$		2.2	–	–	V
Falling Voltage from Power-saving Mode	$V_{PS\ off}$		–	–	0.5	V
Gain Flatness	Flat	f_{IF} ± 2.5 MHz	–	–	Δ0.5	dB

STANDARD CHARACTERISTICS FOR REFERENCE – μPC8190K (RX) – (Unless otherwise specified, V_{CC} = 3.0 V, T_A = +25°C, f_{IF} = 382.5 MHz, f_{LO} = 760 MHz, P_{LO} = –15 dBm, $f_{I/Q}$ = 2.5 MHz)

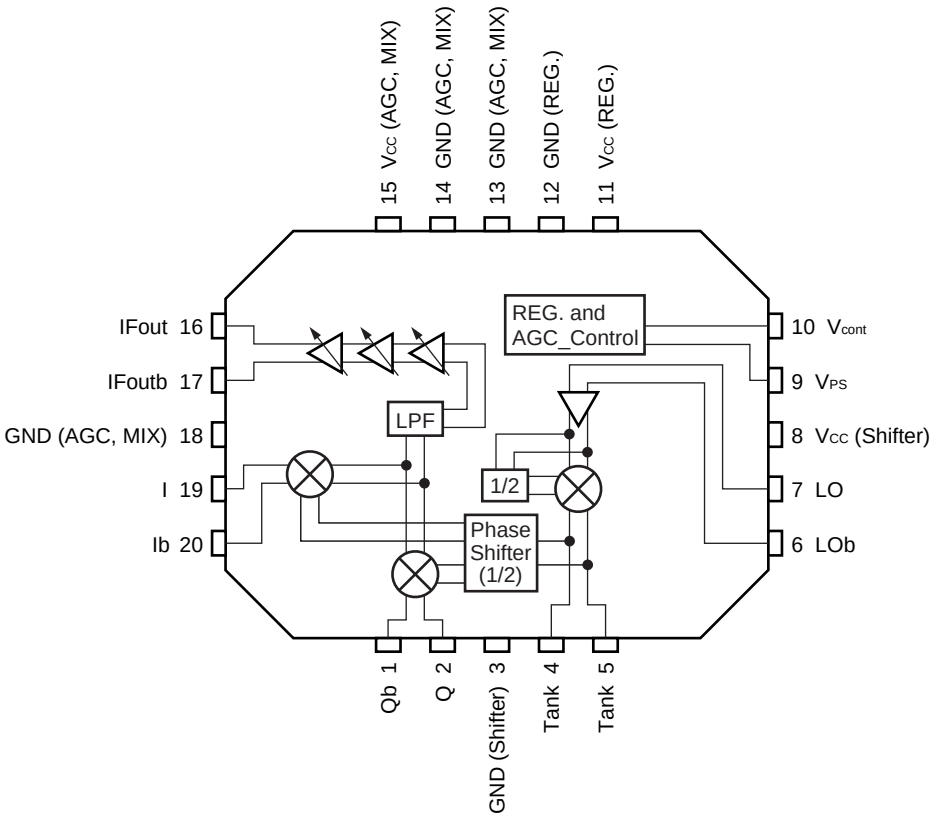
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Noise Figure	NF	Gain = +65 dB	–	9.5	12	dB
Error Vector Magnitude (Vector Error)	EVM	IF = 380 MHz, 3.84 Msps QPSK modulation, gain is adujsted	–	3	–	%rms
Gain 1 dB Compression Input Power	$P_{in\ (1\ dB)}$	Gain = +50 dB	–	–45	–	dBm

MEASUREMENT CIRCUIT – μPC8190K (RX) –

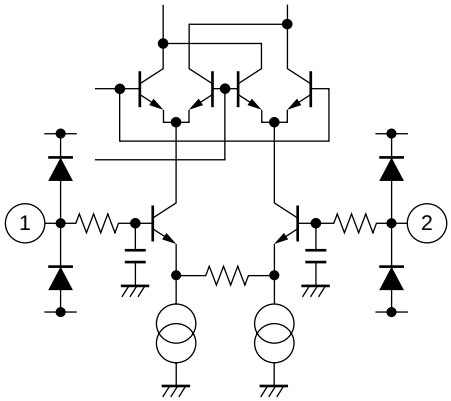
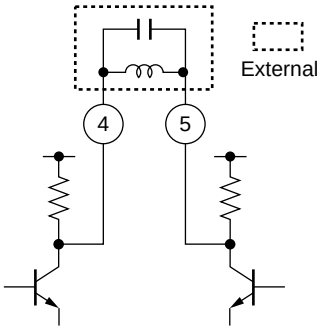
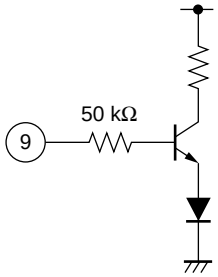


INTERNAL BLOCK DIAGRAM AND PIN CONFIGURATION – μPC8191K (TX) –

(Top View)

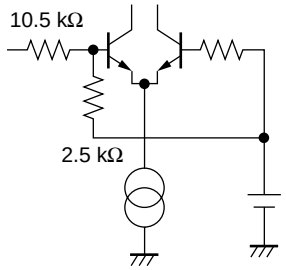
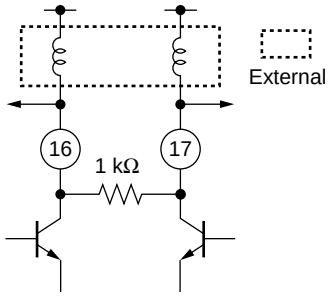
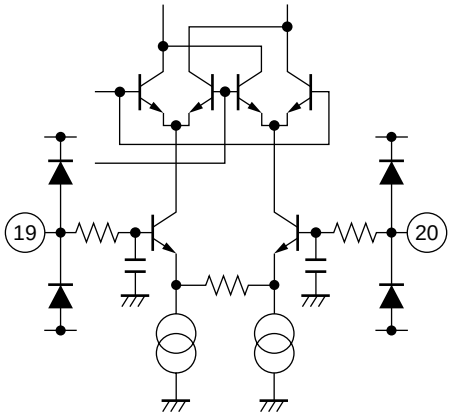


PIN EXPLANATIONS – μPC8191K (TX) –

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (TYP.) (V) Note	Functions and Applications	Internal Equivalent Circuits
1	Qb	V_{CC}/2	–	Q signal input pin. Apply bias voltage externally. Maximum balance input voltage is 1 000 mV_{P-P} (balance).	
2	Q	V_{CC}/2	–		
3	GND (Shifter)	0	–	Ground pin of I/Q modulator. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impedance.	———
4 5	Tank	0	2.65	External inductor and capcitor can supress harmonics spurious of LO frequency. LC value should be determined according to LO input frequency and suppression level.	
6	LOb	0	2.02	Bypass pin of local signal inpu for I/Q modulator. In the case of single local input, this pin must be decoupled with capacitor ex. 1 000 pF.	———
7	LO	0	2.02	Local signal input of I/Q modulator. The DC cut capacitor ex. 1 000 pF must be attaced to this pin.	———
8	V_{CC} (Shifter)	2.7 to 3.3	–	Supply voltage pin of I/Q modulator.	———
9	V_{PS}	0 to 3.0	–	Power saving pin of I/Q modulator + AGC amplifier. This pin modulator can control Active/Sleep state with bias as follows. V_{PS} (V) / State: 0 to 0.5 – Sleep Mode 2.2 to 3 – Active Mode	

Note Pin voltage is measured at V_{CC} = 2.85 V

– μPC8191K (TX) –

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (TYP.) (V) Note	Functions and Applications	Internal Equivalent Circuits
10	V_{cont}	0 to 3.0	–	Gain control pin of AGC amplifier. Variable gains are available in accordance with applied voltage between 0 to 3.0 V.	
11	V_{CC} (REG.)	2.7 to 3.3	–	Supply voltage pin of internal regulator.	———
12	GND (REG.)	0	–	Ground pin internal regulator. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impedance.	———
13 14 18	GND (AGC, MIX)	0	–	Ground pin of AGC amplifier + I/Q Mixer. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impedance.	———
15	V_{CC} (AGC, MIX)	2.7 to 3.3	–	Supply voltage pin of AGC amplifier + I/Q Mixer.	———
16	IFout	2.7 to 3.3	–	IF output pin. The inductor must be attached between V_{CC} and output pin due to open collector. Output frequency is 570 MHz which is 3/4 of local signal frequency 760 MHz.	
17	IFoutb	2.7 to 3.3	–	Balance output of IFout pin. The inductor must be attached between V_{CC} and output pin due to open collector.	
19	I	V_{CC}/2	–	I signal input pin. Apply bias voltage externally. Maximum balance input voltage is 1 000 mV_{P-P} (balance).	
20	Ib	V_{CC}/2	–		

Note Pin voltage is measured at V_{CC} = 2.85 V

ABSOLUTE MAXIMUM RATINGS – μPC8191K (TX) –

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	4.0	V
Applied Voltage	V_{PS}, V_{cont}	–0.3 to V_{CC} + 0.3	V
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	°C

RECOMMENDED OPERATING RANGE – μPC8191K (TX) –

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		2.7	3.0	3.3	V
Operating Ambient Temperature	T_A		–25	25	85	°C
IF Frequency	f_{IF}		–	570	–	MHz
Local Frequency	f_{LO}		–	760	–	MHz
Local Input Level	P_{LO}		–18	–15	–12	dBm
IF Output Impedance	Z_{IF}	Balance output internal resistance	–	1	–	kΩ
I/Q Maximum Input Voltage	$VI_{/Q}$	Balance input	–	0.4	1	V_{P-P}

ELECTRICAL CHARACTERISTICS – μPC8191K (TX) –

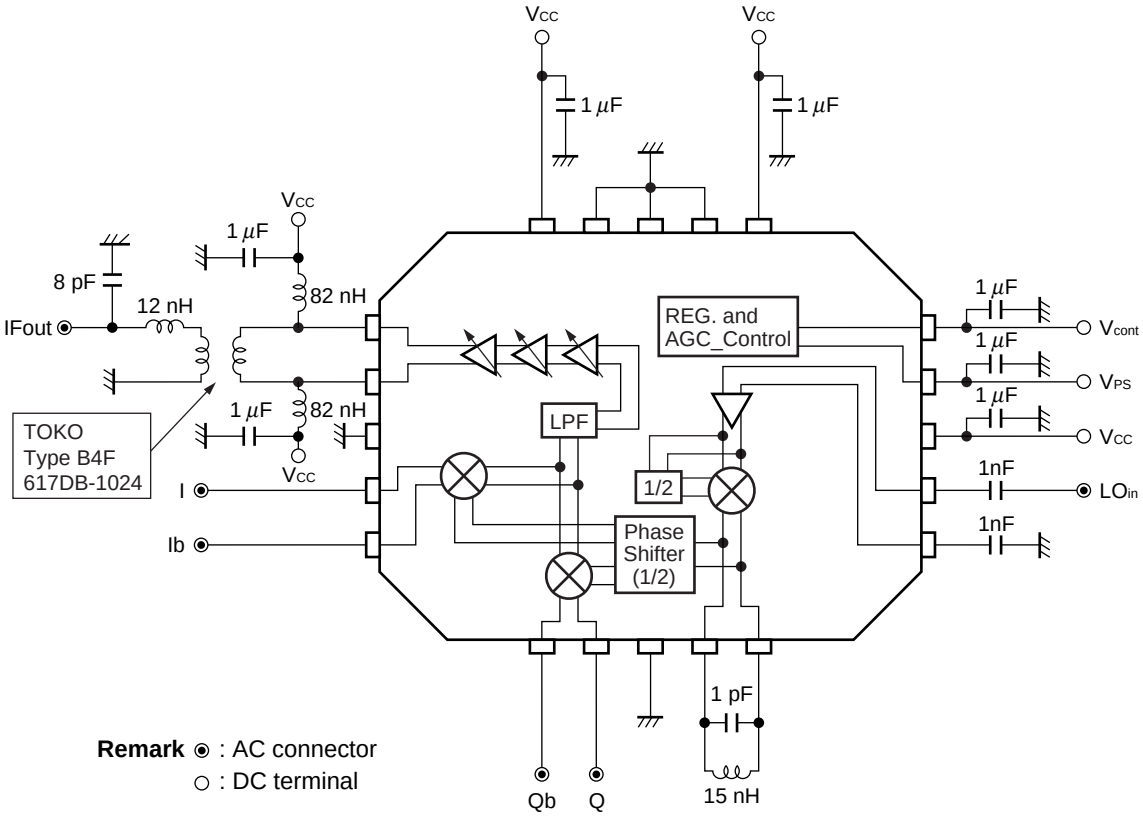
(Unless otherwise specified, V_{CC} = 3.0 V, T_A = +25°C, f_{IF} = 570 MHz, f_{LO} = 760 MHz, P_{LO} = –15 dBm, $f_{I/Q}$ = 10 kHz, 400 mV_{P-P} balanced sine-wave)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No input signal	–	30.5	38	mA
		At power-saving mode	–	0	1	μA
Output Power	P_{out}	V_{cont} = 2.3 V, I/Q = 400mV_{P-P} balanced	–17	–13	–	dBm
		V_{cont} = 0.3 V, I/Q = 400mV_{P-P} balanced	–	–93	–88	dBm
Local Leakage	LOL		–	–	–30	dBc
Image Rejection	ImR		–	–	–30	dBc
Output Harmonics 1	Hm1	Leakage when IF output = 190 MHz	–	–	–20	dBc
Output Harmonics 2	Hm2	Leakage when IF output = 380 MHz	–	–	–30	dBc
Rise Time from Power-saving Mode	t_{PS}		–	–	10	μs
Rising Voltage from Power-saving Mode	$V_{PS\ on}$		–	–	2.2	V
Falling Voltage from Power-saving Mode	$V_{PS\ off}$		0.5	–	–	V

STANDARD CHARACTERISTICS FOR REFERENCE – μPC8191K (TX) –
(Unless otherwise specified, V_{CC} = 3.0 V, T_A = +25°C, f_{IF} = 570 MHz, f_{LO} = 760 MHz, P_{LO} = –15 dBm, $f_{I/Q}$ = 10 kHz, 400 mV_{P-P} balanced sine-wave)

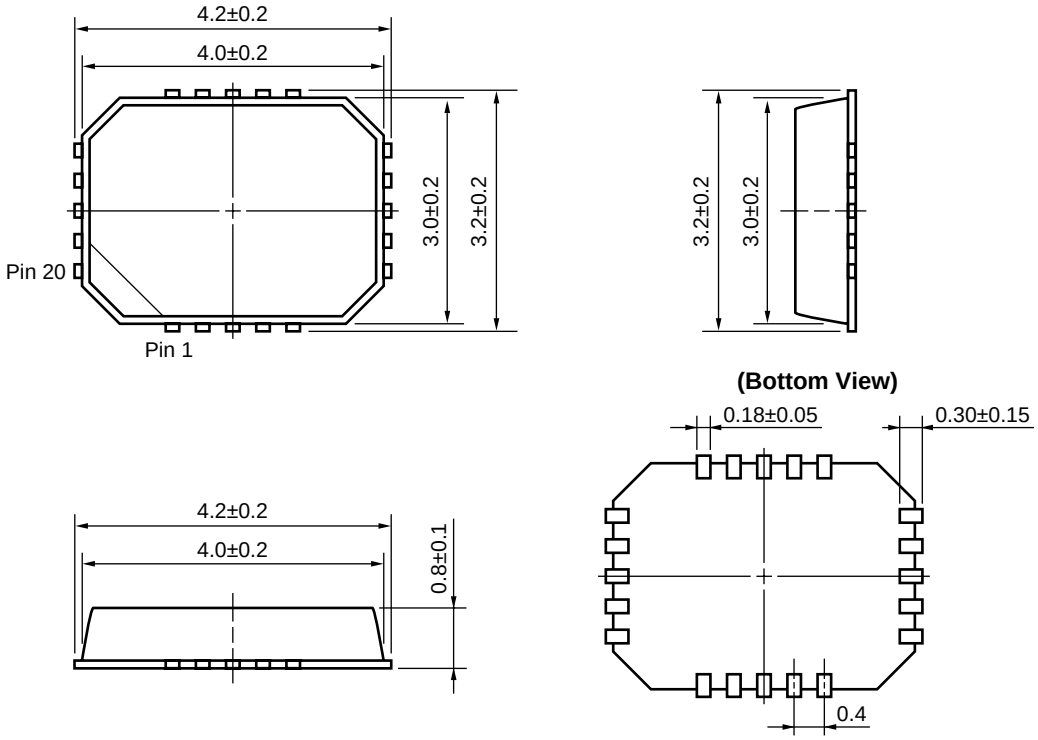
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Output Noise Level 1	NFL1	P_{out} = –25 dBm, f_{IF} ± 20 MHz	–	–148	–	dBm/Hz
Output Noise Level 2	NFL2	P_{out} = –65 dBm, f_{IF} ± 20 MHz	–	–162	–	dBm/Hz
Error Vector Magnitude (Vector Error)	EVM		–	3	–	%rms
Adjacent Channel Power	ACPR	f_{IF} ± 5 MHz	–	–55	–	dBc

MEASUREMENT CIRCUIT – μPC8191K (TX) –



PACKAGE DIMENSIONS

20-PIN PLASTIC QFN (PIN-PITCH: 0.4 mm, UNIT: mm)



NOTE ON CORRECT USE

(1) Observe precautions for handling because this IC is an electrostatic sensitive device.
(2) Form a ground pattern as widely as possible to minimize its impedance (to prevent undesires oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor to the V_{CC} pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below, Time: 30 seconds or less (at 210°C or higher), Count: 3 times or less, Exposure limit: None[Note]	IR35-00-3
VPS	Package peak temperature: 215°C or below, Time: 40 seconds or less (at 200°C or higher), Count: 3 times or less, Exposure limit: None[Note]	VP15-00-3
Partial Heating	Pin temperature: 300°C or below, Time: 3 seconds or less (per side of device), Exposure limit: None[Note]	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For the details the recommended soldering conditions, refer to the document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

[MEMO]

[MEMO]

[MEMO]

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