NEC

MOS INTEGRATED CIRCUIT
μPD16306B

64-BIT HIGH WITHSTAND VOLTAGE CMOS DRIVER

DESCRIPTION

The μPD16306B is a high withstand voltage CMOS driver for flat display panels such as PDP, VFD and EL. It consists of a 64-bit bi-directional shift register, a 64-bit latch and a high withstand voltage CMOS driver. The logic circuit operates on 5 V power supply (CMOS level input), so that it can be connected to a microcomputer. The driver block comprises 80 V, 50 mA MAX. high withstand voltage output buffer, and both the logic block and driver block consist of CMOS, allowing operation with low power consumption.

FEATURES

- 64-bit bi-directional shift registers
- Data control by transfer clock (external) and latch
- High-speed data transfer: $f_{MAX.}$ = 16 MHz MIN. (in cascade connection)
- Wide operating temperature range: T_A = –40 to +85 °C
- High withstand voltage output: 80 V, 50 mA MAX.
- High withstand voltage Full CMOS process
- Polarities of all drivers can be reversed by using /PC pin.

Remark /xxx indicates active low signal.

ORDERING INFORMATION

Part Number	Package
μPD16306BGF-3BA	100-pin plastic QFP (14 x 20)

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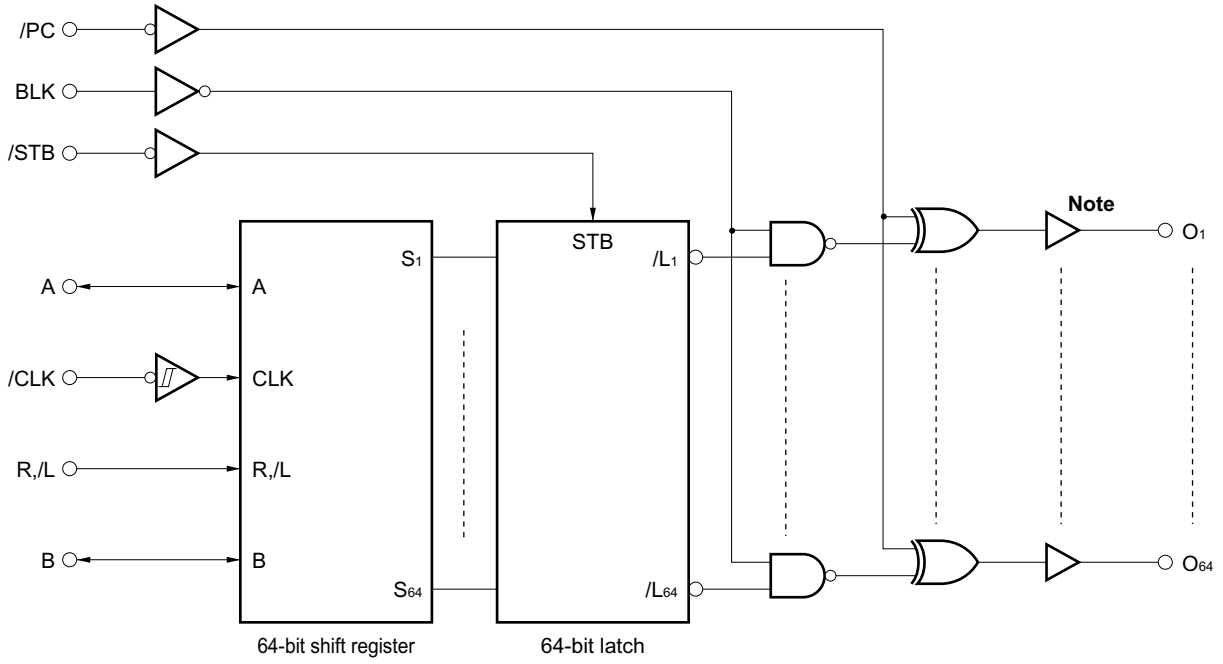
The mark ★ shows major revised points.

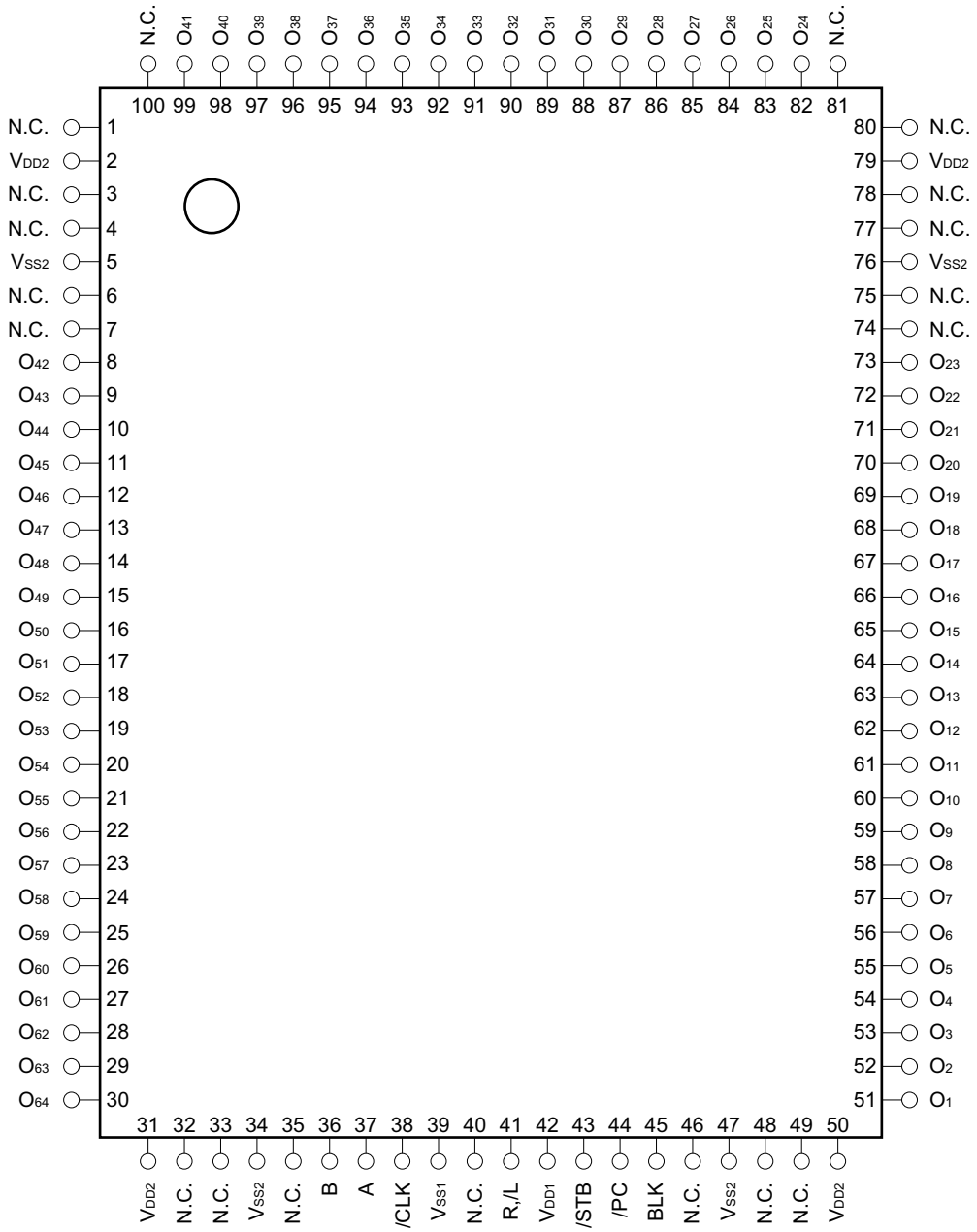
1. BLOCK DIAGRAM



Note High withstand voltage CMOS drivers (80 V, ±50 mA MAX.)

2. PIN CONFIGURATION (Top View)

μPD16306BGF-3BA: 100-pin plastic QFP (14 x 20)



Cautions 1. Be sure to leave pin 40 open because it is connected to the lead frame.

2. Be sure to use all the V_{DD1}, V_{DD2}, V_{SS1} and V_{SS2} pins. Keep the V_{SS1} and V_{SS2} pins at the same voltage level.

3. Supply power to V_{DD1}, logic inputs and V_{DD2} in this order to protect the device from destruction due to latch up. Turn off power in the reverse order.
Observe these power sequences even during a transition period.

4. Since the μPD16306B have a CMOS structure, be careful about electrical static destruction.

3. PIN FUNCTIONS

Pin Symbol	Pin Name	I/O	Remark
/PC	Polarity reverse	Input	/PC = L: Reverses polarities of all outputs
BLK	Blank	Input	BLK = H: All outputs = H or L
/STB	Latch strobe	Input	Through at L, holds data at H
A	RIGHT data	I/O	R,/L = H: A input, B output
B	LEFT data	I/O	R,/L = L: B input, A output
/CLK	Clock	Input	Executes shift at falling edge
R,/L	Shift direction control	Input	Right shift mode at H: A → O_1...O_{64} →B Left shift mode at L: B → O_{64}...O_1 → A
O_1 to O_{64}	High withstand voltage output	Output	80 V, 50 mA MAX.
V_{DD1}	Logic power supply	–	5 V ± 10%
V_{DD2}	Driver power supply	–	10 to 70 V
V_{SS1}	Logic ground	–	Connected to GND of system
V_{SS2}	Power ground	–	Connected to GND of system
N.C.	Non connection	–	No connection. Be sure to leave pin 40 open.

4. TRUTH TABLE

Shift Register

Input		I/O		Shift Register
R,/L	/CLK	A	B	
H	↓	Input	Output Note1	Right shift
H	H or L		Output	Hold
L	↓	Output Note2	Input	Left shift
L	H or L	Output		Hold

Notes 1. S_{63} is shifted to the position of S_{64} and output from B at the falling edge of the clock.

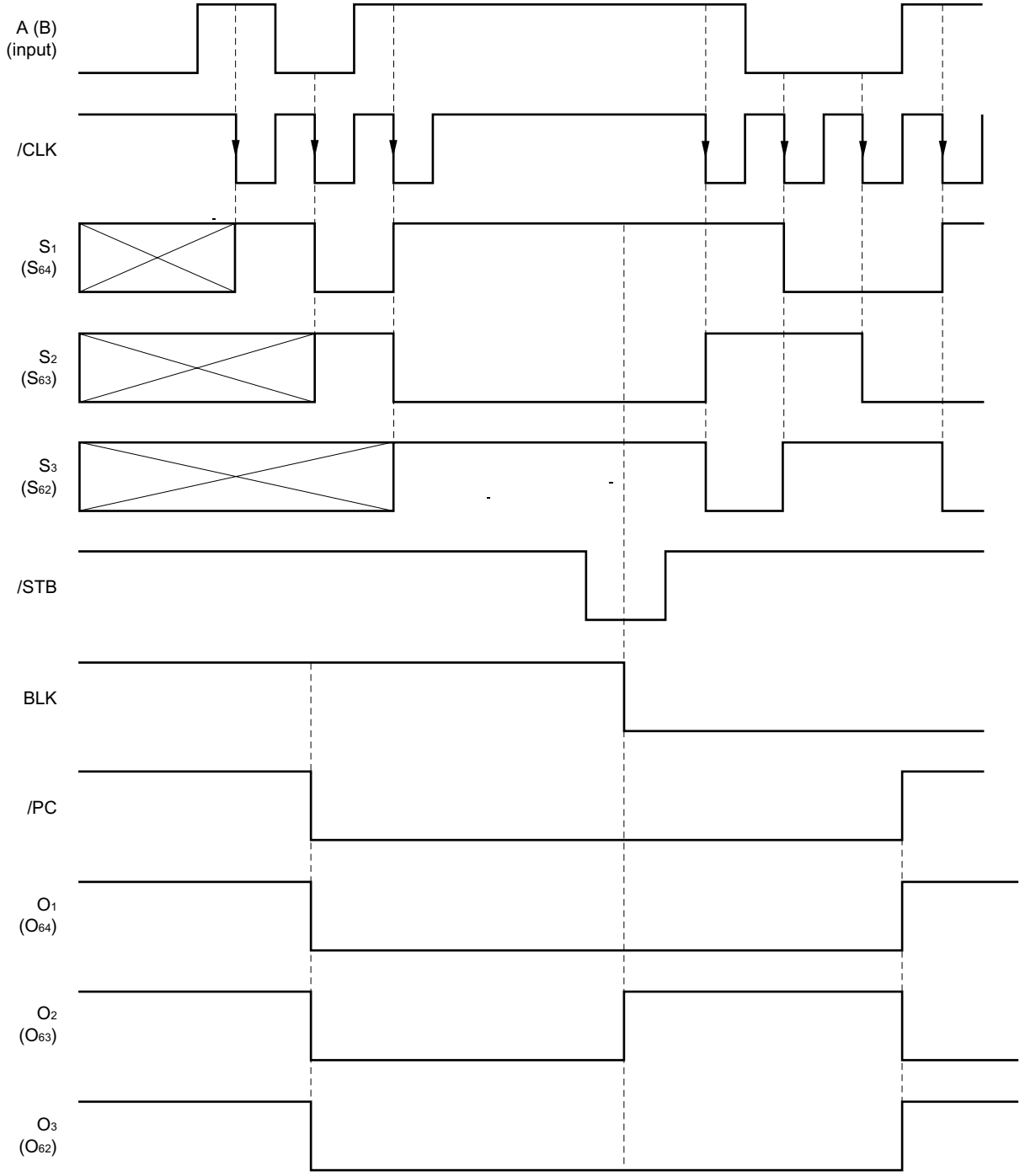
2. S_2 is shifted to the position of S_1 and output from A at the falling edge of the clock.

Latch and Driver

Input				Driver Output Stage
A (B)	/STB	BLK	/PC	
X	X	H	H	H (All driver outputs are H.)
X	X	H	L	L (All driver outputs are L.)
H	L	L	H	H
H	L	L	L	L
L	L	L	H	L
L	L	L	L	H
X	H	L	H	Outputs data immediately before the /STB goes to H.
X	H	L	L	Reverses and outputs data immediately before the /STB goes to H.

Remark X = H or L, H = high level, L = low level

5. TIMING CHART



Remark ( ): R,/L = L

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD1}	−0.5 to +7.0	V
Logic input voltage	V_{I1}	−0.5 to V_{DD1} + 0.5	V
Logic output voltage	V_{O1}	−0.5 to V_{DD1} + 0.5	V
Driver supply voltage	V_{DD2}	−0.5 to +80	V
Driver output voltage	V_{O2}	−0.5 to V_{DD2} + 0.5	V
Driver output current	I_{O2}	±50	mA
Power dissipation	P_D	1000	mW
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –40 to +85°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}	4.5	5.0	5.5	V
High-level input voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low-level input voltage	V_{IL}	0		0.2 V_{DD1}	V
Driver supply voltage	V_{DD2}	10		70	V
Driver output current	I_{OL2}			+40	mA
	I_{OH2}			−40	mA

Electrical Characteristics (T_A = 25°C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH1}	Logic I_{OH1} = –1.0 mA	0.9 V_{DD1}			V
Low-level output voltage	V_{OL1}	Logic I_{OL1} = 1.0 mA			0.1 V_{DD1}	V
High-level output voltage	V_{OH21}	O_1 to O_{64}, I_{OH2} = –1.0 mA	69			V
	V_{OH22}	O_1 to O_{64}, I_{OH2} = –10.0 mA	65			V
Low-level output voltage	V_{OL21}	O_1 to O_{64}, I_{OL2} = 5.0 mA			1.0	V
	V_{OL22}	O_1 to O_{64}, I_{OL2} = 40.0 mA			10	V
High-level input voltage	V_{IH}	Logic	0.7 V_{DD1}			V
Low-level input voltage	V_{IL}	Logic			0.2 V_{DD1}	V
High-level input current	I_{IH}	V_I = V_{DD1}			1.0	μA
Low-level input current	I_{IL}	V_I = 0 V			–1.0	μA
Static current dissipation	I_{DD11}	Logic, T_A = 25°C			10	μA
	I_{DD12}	Logic, T_A = –40 to +85°C			100	μA
	I_{DD21}	Driver, T_A = 25°C			100	μA
	I_{DD22}	Driver, T_A = –40 to +85°C			1000	μA

Switching Characteristics (T_A = 25°C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V, Logic: C_L = 15 pF, Driver: C_L = 50 pF)

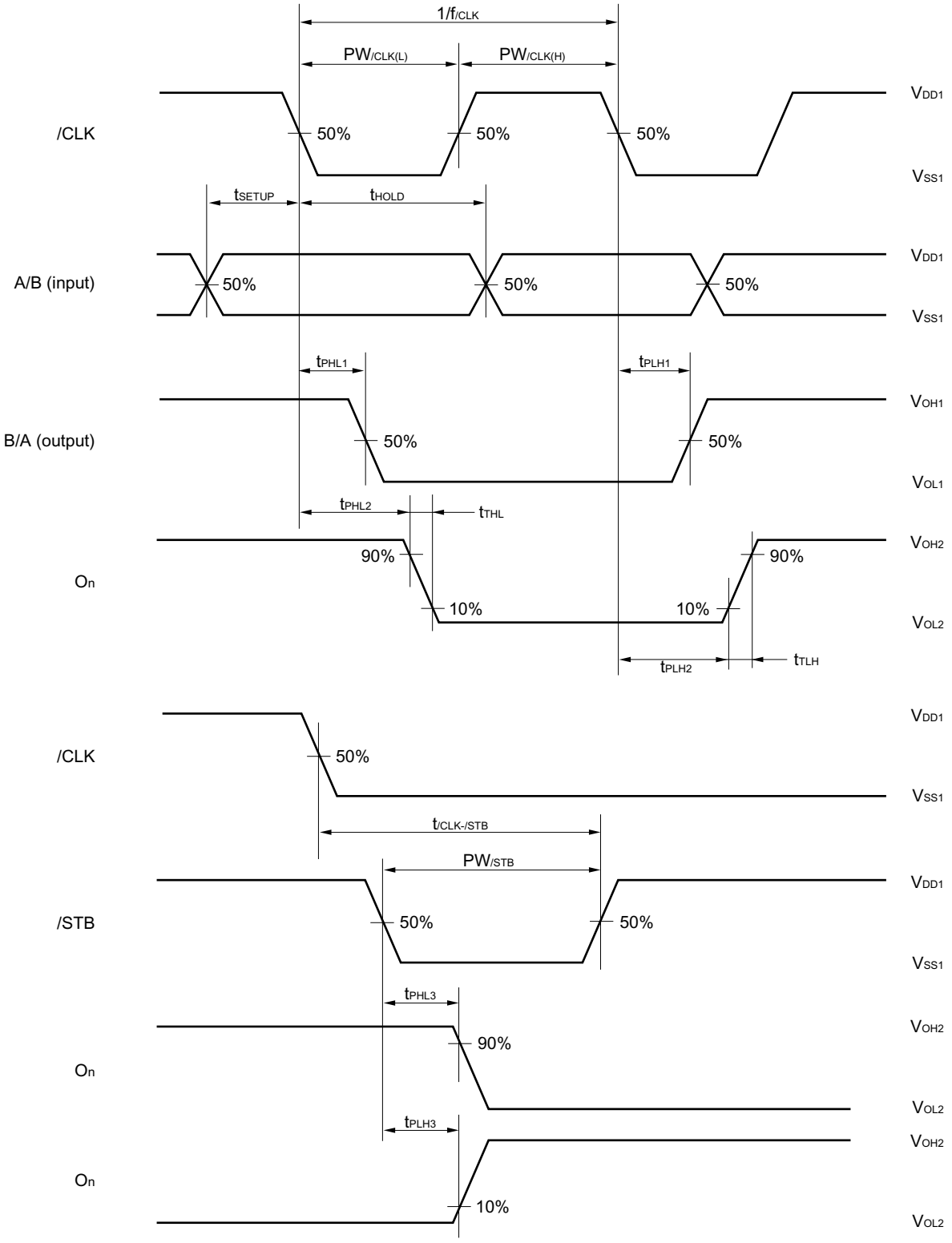
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Propagation delay time	t_{PHL1}	/CLK → A/B			50	ns
	t_{PLH1}				50	ns
	t_{PHL2}	/CLK → O_1 to O_{64}			160	ns
	t_{PLH2}				160	ns
	t_{PHL3}	/STB → O_1 to O_{64}			150	ns
	t_{PLH3}				150	ns
	t_{PHL4}	BLK → O_1 to O_{64}			145	ns
	t_{PLH4}				145	ns
	t_{PHL5}	/PC → O_1 to O_{64}			140	ns
	t_{PLH5}				140	ns
Rise time	t_{TLH}	O_1 to O_{64}			100	ns
Fall time	t_{THL}	O_1 to O_{64}			100	ns
Maximum clock frequency	$f_{MAX.}$	Duty = 50%, data loading	20			MHz
		In cascade connection	16			MHz
Input capacitance	C_I				20	pF

Timing Requirements (T_A = –40 to +85°C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock pulse width	$PW_{/CLK(L)}$, $PW_{/CLK(H)}$		20			ns
Strobe pulse width	$PW_{/STB}$		20			ns
Blank pulse width	PW_{BLK}		200			ns
/PC pulse width	$PW_{/PC}$		200			ns
Data setup time	t_{SETUP}		10			ns
Data hold time	t_{HOLD}		10			ns
Clock-strobe time	$t_{/CLK-/STB}$	/CLK ↓ → /STB ↑	50			ns

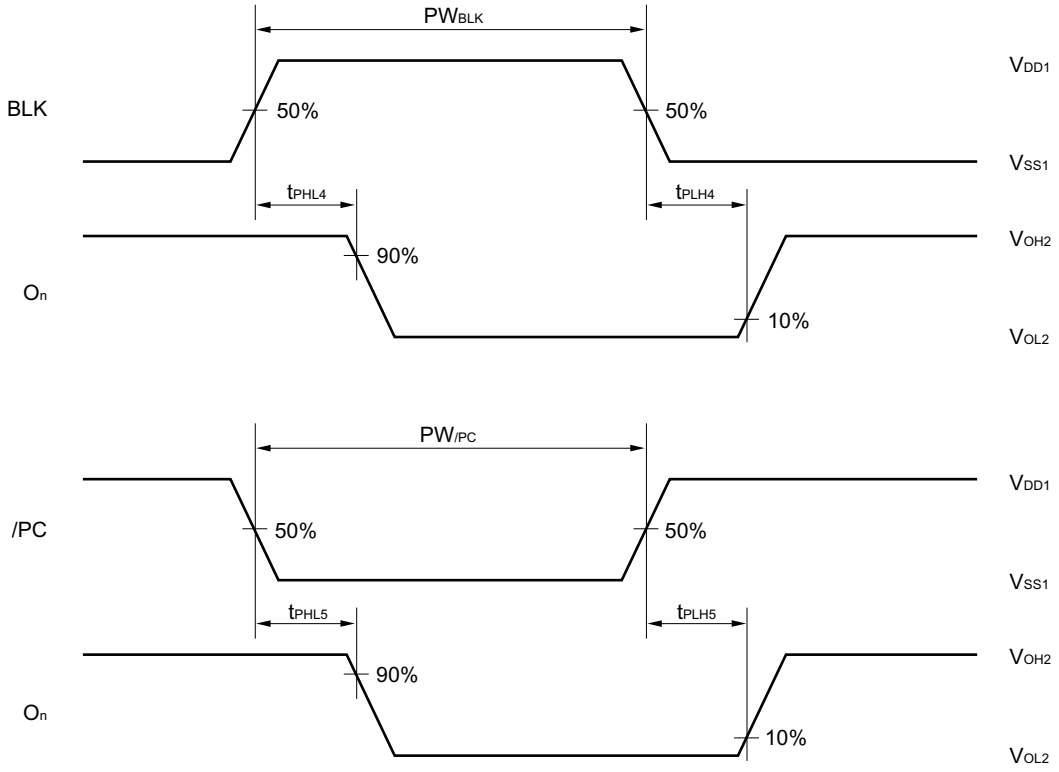
Switching Characteristics Waveforms (1/2)

Unless otherwise specified, $V_{IH} = V_{IL} = 0.5\ V_{DD1}$.



Switching Characteristics Waveforms (2/2)

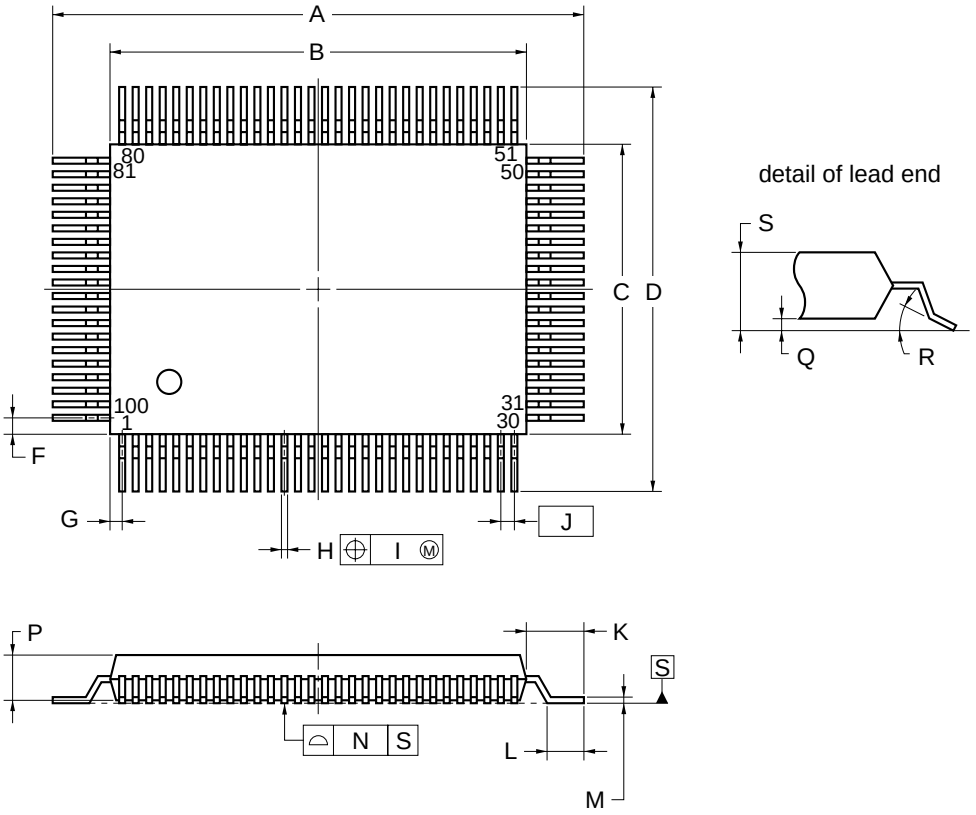
Unless otherwise specified, $V_{IH} = V_{IL} = 0.5\ V_{DD1}$.



★ 7. PACKAGE DRAWING

μPD16306BGF-3BA

100-PIN PLASTIC QFP (14x20)



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.6±0.4
B	20.0±0.2
C	14.0±0.2
D	17.6±0.4
F	0.8
G	0.6
H	0.30±0.10
I	0.15
J	0.65 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

P100GF-65-3BA-4

★ 8. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16306B.
For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**
Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Type of Surface Mount Device

μPD16306BGF-3BA: 100-pin plastic QFP (14 x 20)

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235°C or below, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: MAX. 3	IR35-00-3
VPS	Peak temperature of package surface: 215°C or below, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: MAX. 1	VP15-00-1
Partial heating method	Terminal temperature: 300°C or below, Time: 3 seconds or below (Per one side of the device).	–

Caution Do not apply more than one soldering method at any one time, except for the partial heating method.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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