NEC

MOS INTEGRATED CIRCUIT

μPD16327

64-BIT AC-PDP DRIVER

The μPD16327 is a high breakdown voltage CMOS driver for flat display panels such as PDP, VFD and EL. It consists of 64-bit bidirectional shift registers (16 bits × 4 circuits), a 64-bit latch, and a high breakdown voltage CMOS driver. The logic block operates on a 5 V power supply, designed to be connected directly to a microcomputer (CMOS level input). The driver block comprises 100 V, 40 mA MAX. high breakdown voltage output, and both the logic block and driver block consist of CMOS, allowing operation with low power consumption.

FEATURES

- 4 circuits of 16-bit bidirectional shift registers on chip
- Data control by transfer lock (external) and latch
- High-speed data transfer capability ($f_{max.}$ = 20 MHz MIN.: With cascading)
- Wide operating temperature range (T_A = –40 to 85 °C)
- High breakdown voltage (100 V, 40 mA MAX.)
- High breakdown voltage CMOS structure
- $\overline{PC}$ pin allows polarity of all driver outputs to be inverted.

ORDERING INFORMATION

Part Number	Package
μPD16327GF-3BA	100-pin plastic QFP

Document No. S10949EJ1V1DS00 (1st edition)
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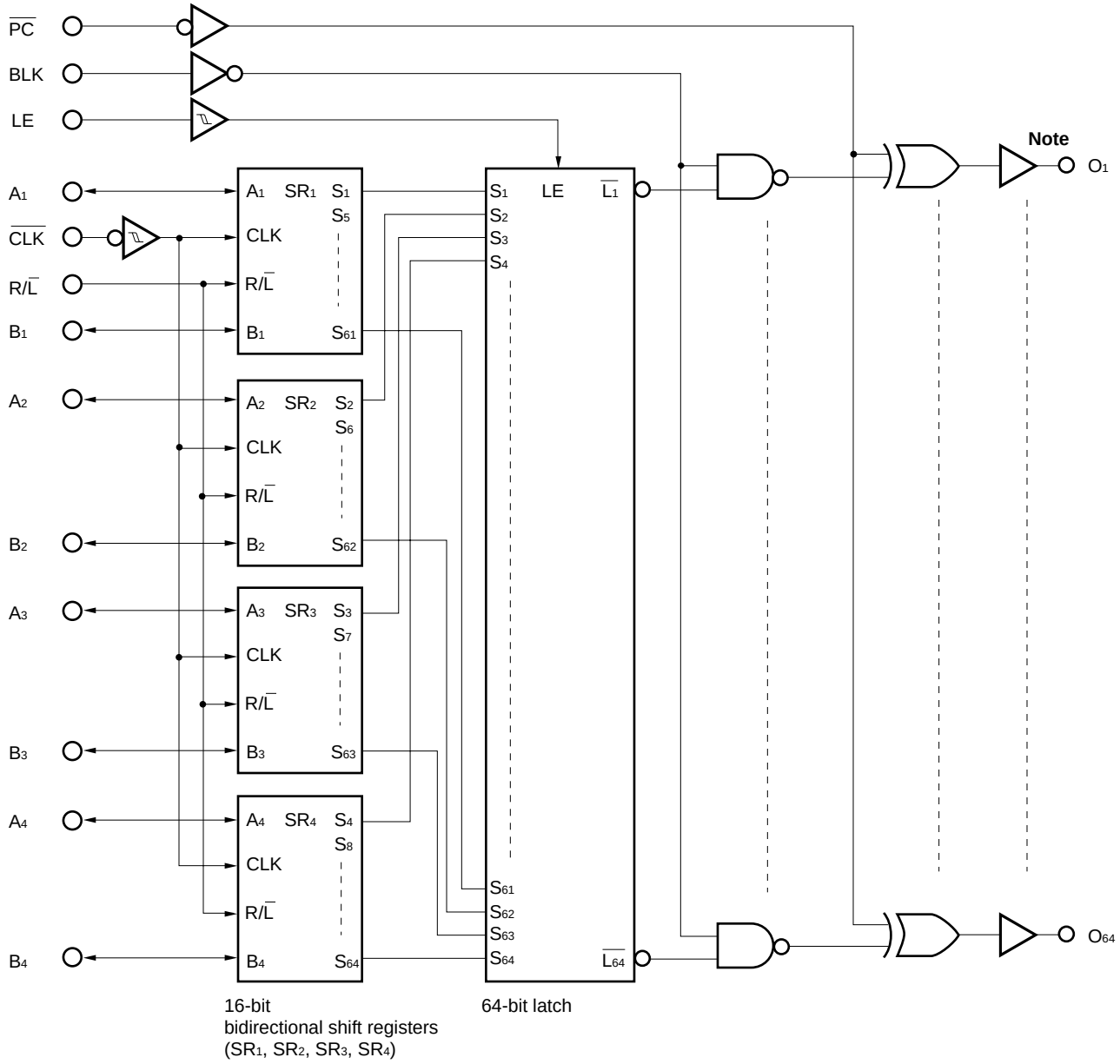
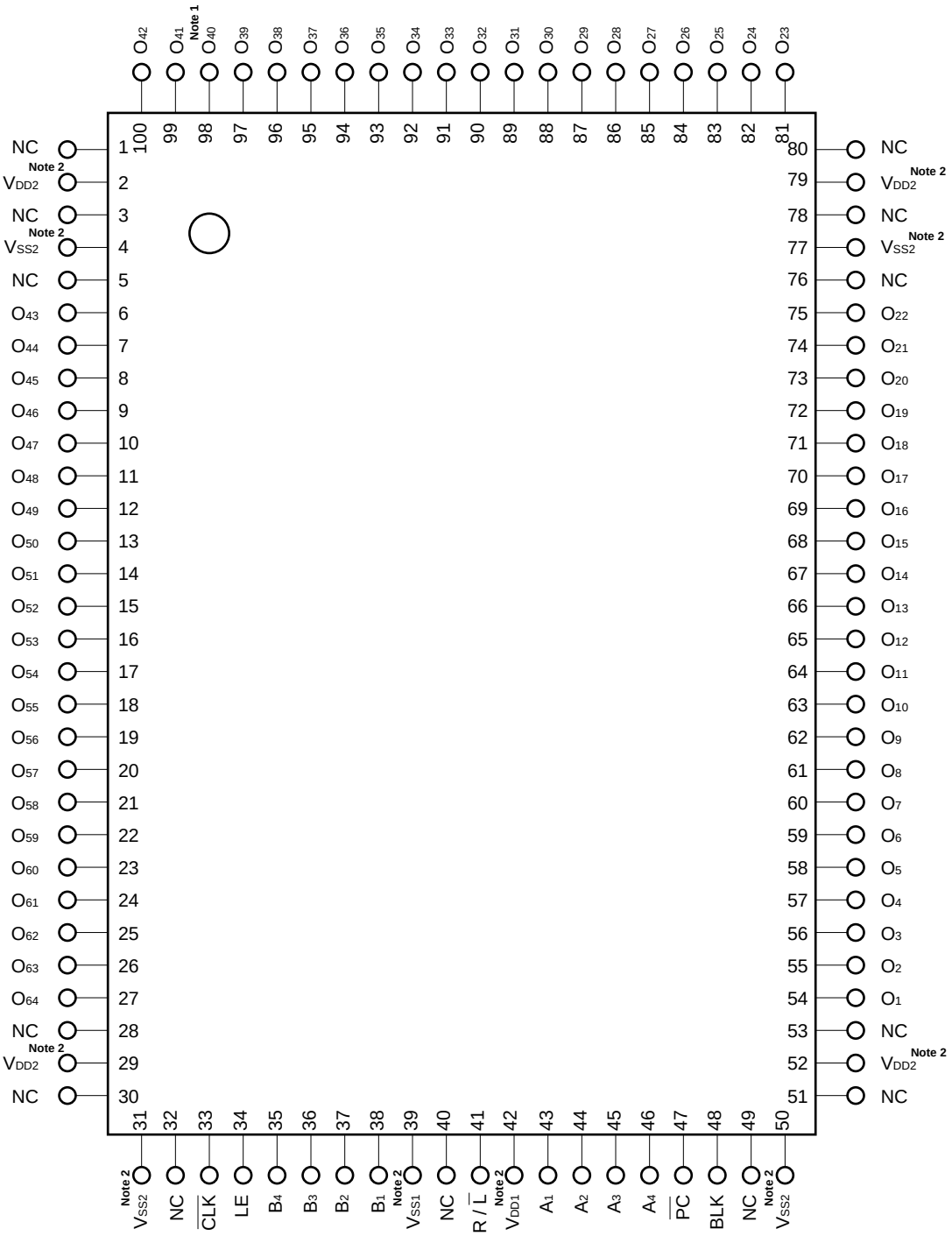
Printed in Japan

BLOCK DIAGRAM



Note High breakdown voltage CMOS driver 100 V ± 40 mA MAX.

PIN CONFIGURATION (Top View)



Notes 1. Be sure to use all pins V_{DD1}, V_{DD2}, V_{SS1} and V_{SS2}. Use V_{SS1} and V_{SS2} at the same potential.

2. Pin 40 is connected to the lead frame, and therefore be sure to leave it open.

Remark In order to prevent latch-up breakage, be sure to enter the power to V_{DD1}, logic signal, and V_{DD2}, in that order, and turn off the power in the reverse order. Keep this order also during a transition period.

PIN DESCRIPTION

Pin Symbol	Pin Name	Pin Number	Description
$\overline{PC}$	Polarity inverted input	47	$\overline{PC}$ = L: Polarity of all outputs inverted
BLK	Blanking input	48	BLK = H: All outputs = H or L
LE	Latch enable input	34	Latch is automatically executed by being driven high upon a clock rise.
A_1 to A_4	RIGHT data input/output	43-46	When R/$\overline{L}$ = H, A_1 to A_4: Input B_1 to B_4: Output When R/$\overline{L}$ = L, A_1 to A_4: Output B_1 to B_4: Input
B_1 to B_4	LEFT data input/output	38-35	
$\overline{CLK}$	Clock input	33	Shift is executed on a fall.
R/$\overline{L}$	Shift control input	41	H: Right shift mode SR_1: $A_1 \rightarrow S_1 \cdots S_{61} \rightarrow B_1$ (SR_2, SR_3, SR_4 also same direction) L: Left shift mode SR_1: $B_1 \rightarrow S_{61} \cdots S_1 \rightarrow A_1$ (SR_2, SR_3, SR_4 also same direction)
O_1 to O_{64}	High breakdown voltage output	54-75, 82-99, 5-28	100 V, 40 mA MAX.
V_{DD1}	Logic block power supply	42	5 V ± 10 %
V_{DD2}	Driver block power supply	2, 30, 51, 79	30 to 150 V
V_{SS1}	Logic ground	39	Connected to system GND
V_{SS2}	Driver ground	4, 32, 49, 77	Connected to system GND
NC	Free pins	1, 3, 5, 29, 31, 40 50, 52, 76, 78, 80 81, 100	Non-connection Be sure to leave pin 40 open.

TRUTH TABLE 1 (SHIFT REGISTER BLOCK)

Input		Output		Shift Register
R/$\overline{L}$	$\overline{CLK}$	A	B	
H	↓	Input	Output[Note 1]	Execution of right shift
H	H or L		Output	Retained
L	↓	Output[Note 2]	Input	Execution of left shift
L	H or L	Output		Retained

Notes 1. On a clock fall, the data items of S_{57}, S_{58}, S_{59} and S_{60} are shifted to S_{61}, S_{62}, S_{63} and S_{64}, and output from B_{61}, B_{62}, B_{63} and B_{64}, respectively.

2. On a clock fall, the data items of S_5, S_6, S_7 and S_8 are shifted to S_1, S_2, S_3 and S_4, and output from A_1, A_2, A_3 and A_4, respectively.

TRUTH TABLE 2 (LATCH BLOCK)

LE	$\overline{CLK}$	Output state of latch block ($\overline{L_n}$)
H	↑	Latches S_n data and retains output data.
	↓	Retains latch data.
L	×	Retains latch data.

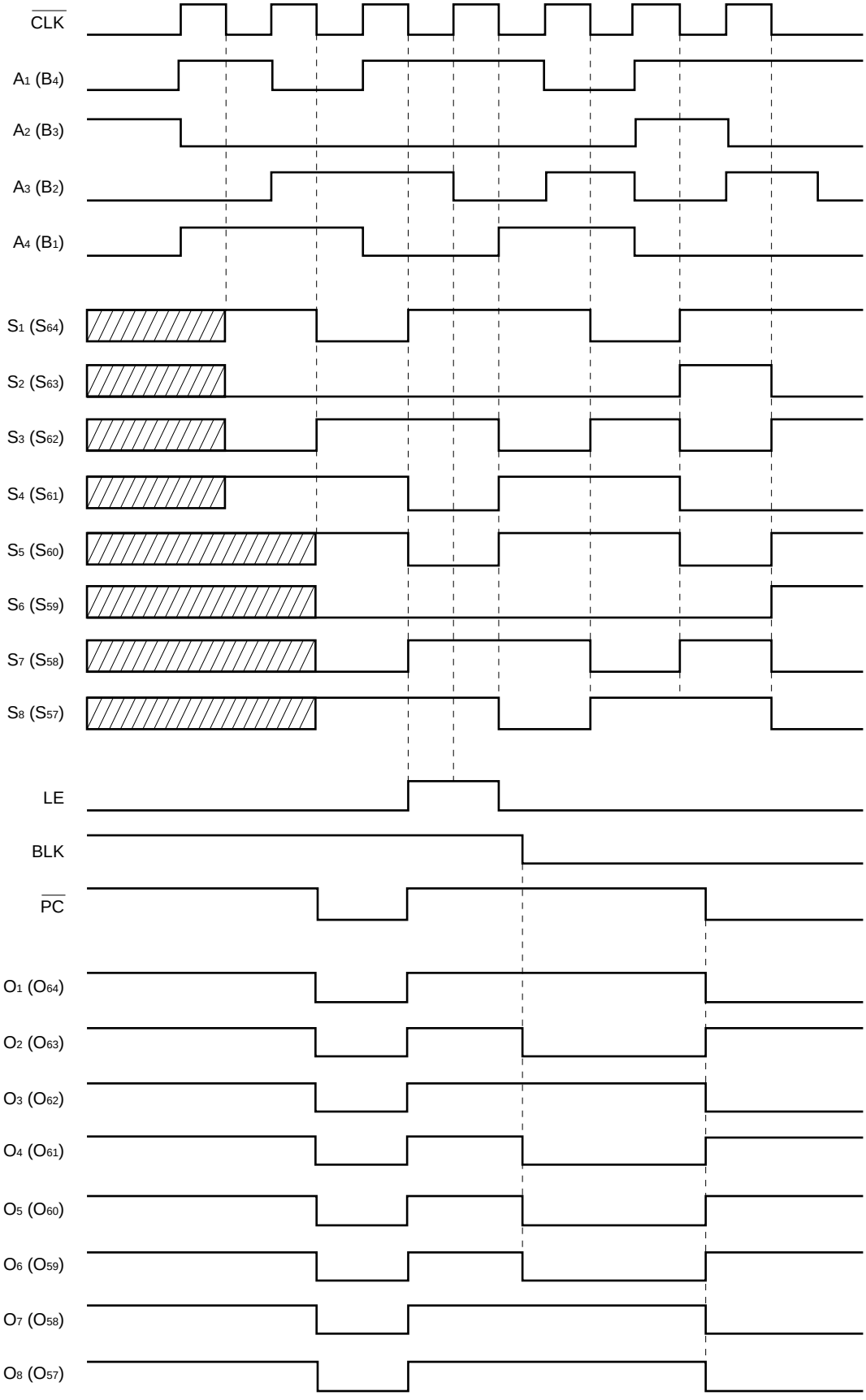
TRUTH TABLE 3 (DRIVER BLOCK)

$\overline{L_n}$	BLK	$\overline{PC}$	Driver output state
×	H	H	H (all driver outputs: H)
×	H	L	L (all driver outputs: L)
×	L	H	Outputs latch data ($\overline{L_n}$).
×	L	L	Outputs latch data ($\overline{L_n}$) with polarity inverted.

Remark X = H or L, H = high level, L = low level

TIMING CHART (RIGHT SHIFT)

( ) applies when R/$\overline{L}$ = L.



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	Rating	Unit
Logic block supply voltage	V_{DD1}	–0.5 to +7.0	V
Driver block supply voltage	V_{DD2}	–0.5 to +100	V
Logic block input voltage	V_I	–0.5 to V_{DD1} + 0.5	V
Driver block output current	I_{O2}	40	mA
Input current	I_I	±25	mA
Package allowable power dissipation	P_D	1300[Note]	mW
Operating ambient temperature	T_A	–40 to +85 °C	°C
Storage temperature	$T_{stg.}$	–65 to +150 °C	°C

Note When $T_A \geq 25$ °C, load should be alleviated at a rate of –13.0 mW/°C.

RECOMMENDED OPERATING RANGE (T_A = –40 to +85 °C, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	MIN.	TYP.	MAX.	Unit
Logic block supply voltage	V_{DD1}	4.5	5.0	5.5	V
Driver block supply voltage	V_{DD2}	30		90	V
Input voltage high	V_{IH}	0.7·V_{DD1}		V_{DD1}	V
Input voltage low	V_{IL}	0		0.2·V_{DD1}	V
Driver output current	I_{OH2}			–30	mA
	I_{OL2}			+30	mA

ELECTRICAL SPECIFICATIONS (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 90 V, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high	V_{OH1}	Logic, I_{OH1}= –1.0 mA	0.9·V_{DD1}		V_{DD1}	V
Output voltage low	V_{OL1}	Logic, I_{OL1}= 1.0 mA	0		0.1·V_{DD1}	V
Output voltage high	V_{OH21}	O_1 to O_{64}, I_{OH2} = –10 mA	83			V
	V_{OH22}	O_1 to O_{64}, I_{OH2} = –30 mA	70			V
Output voltage low	V_{OL21}	O_1 to O_{64}, I_{OL2} = 10 mA			5.0	V
	V_{OL22}	O_1 to O_{64}, I_{OL2} = 30 mA			15	V
Input leakage current	I_{IL}	V_I = V_{DD1} or V_{SS1}			±1.0	μA
Input voltage high	V_{IH}		0.7·V_{DD1}			V
Input voltage low	V_{IL}				0.2·V_{DD1}	V
Static consumption current	I_{DD1}	Logic, T_A = –40 to +85 °C			100	μA
	I_{DD1}	Logic, T_A = 25 °C			10	μA
	I_{DD2}	Driver, T_A = –40 to +85 °C			1000	μA
	I_{DD2}	Driver, T_A = 25 °C			100	μA

SWITCHING CHARACTERISTICS (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 90 V, V_{SS1} = V_{SS2} = 0 V, logic C_L = 15 pF, driver C_L = 50 pF, t_r = t_f = 6.0 ns)

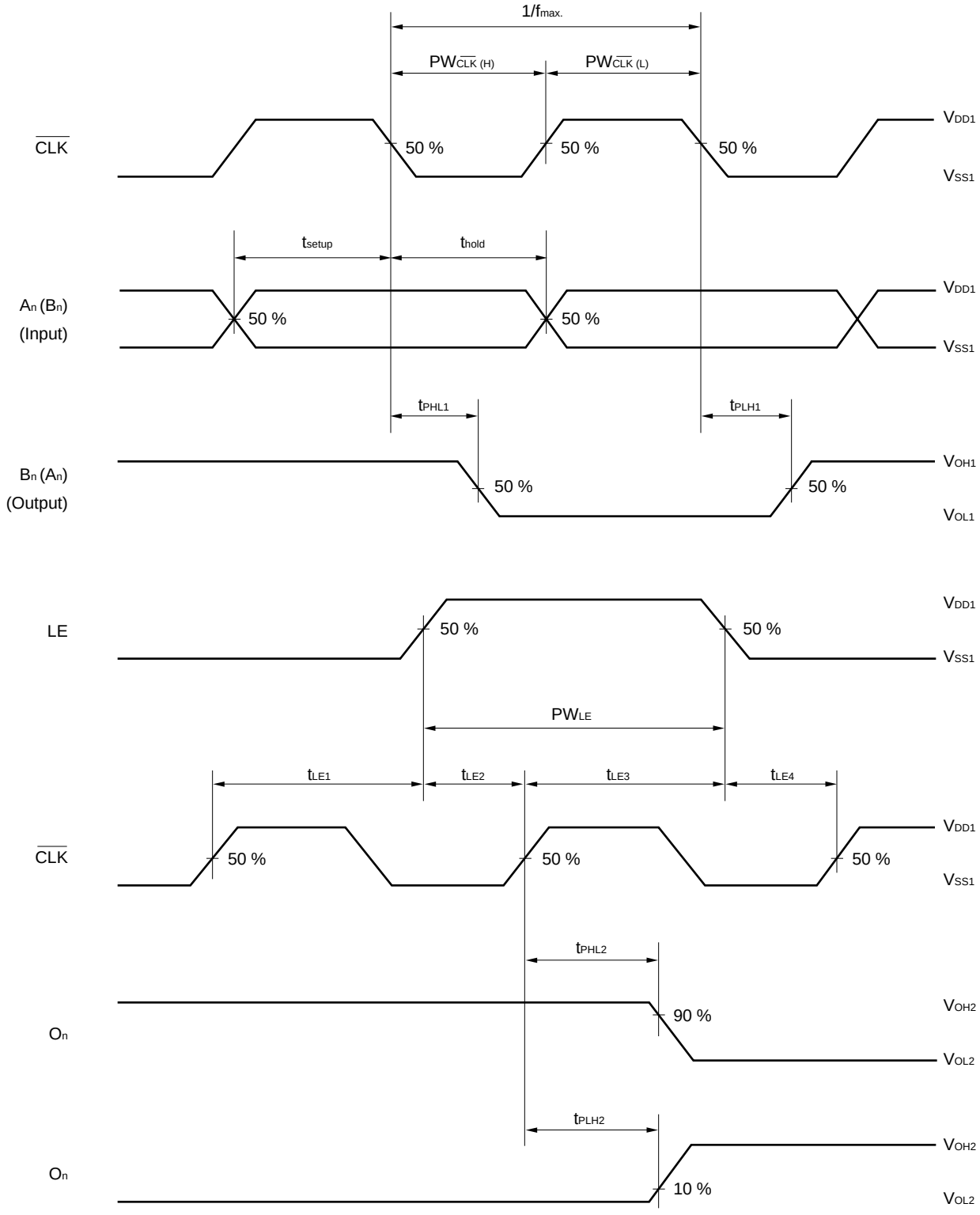
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmission delay time	t_{PHL1}	$\overline{CLK}$ ↓ → A/B			40	ns
	t_{PLH1}				40	ns
	t_{PHL2}	$\overline{CLK}$ ↑ (LE = H) → O_1 to O_{64}			180	ns
	t_{PLH2}				180	ns
	t_{PHL3}	BLK → O_1 to O_{64}			165	ns
	t_{PLH3}				165	ns
	t_{PHL4}	$\overline{PC}$ → O_1 to O_{64}			160	ns
	t_{PLH4}				160	ns
Rise time	t_{TLH}	O_1 to O_{64}			200	ns
Fall time	t_{THL}	O_1 to O_{64}			200	ns
Maximum clock frequency	$f_{max.}$	Data fetch, Duty = 50 % T_A = –40 to 85 °C V_{DD1} = 4.5 to 5.5 V	25			MHz
		With cascading, Duty = 50 % T_A = –40 to 85 °C V_{DD1} = 4.5 to 5.5 V	20			MHz
Input capacitance	C_I				15	pF

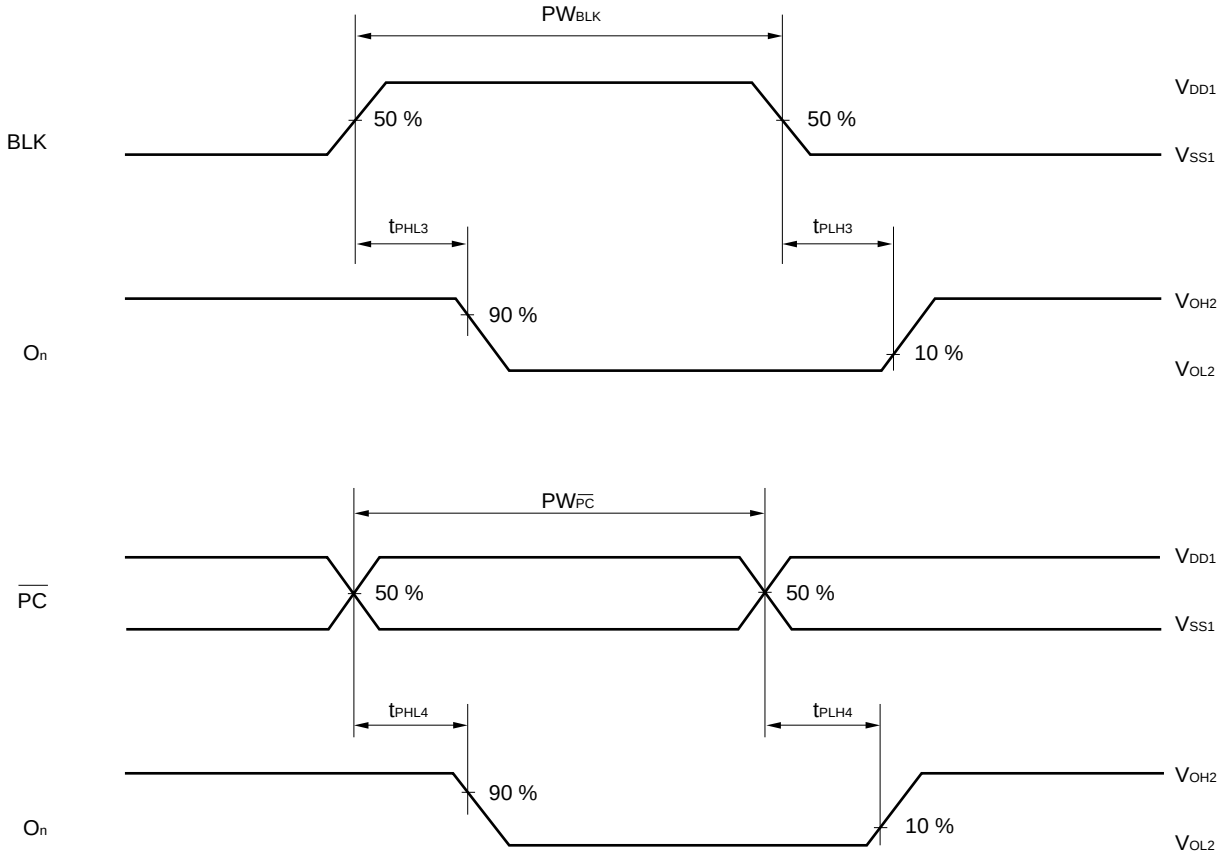
TIMING REQUIREMENTS (T_A = –40 to +85 °C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 6.0 ns)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	$PW_{\overline{CLK}}$		20			ns
Latch enable pulse width	PW_{LE}		30			ns
Blank pulse width	PW_{BLK}		500			ns
$\overline{PC}$ pulse width	$PW_{\overline{PC}}$		500			ns
Data setup time	t_{setup}		10			ns
Data hold time	t_{hold}		10			ns
Latch enable time 1	t_{LE1}		20			ns
Latch enable time 2	t_{LE2}		10			ns
Latch enable time 3	t_{LE3}		20			ns
Latch enable time 4	t_{LE4}		10			ns

SWITCHING CHARACTERISTIC WAVEFORM (R/$\overline{L}$ = H)

( ) applies when R/$\overline{L}$ = L.

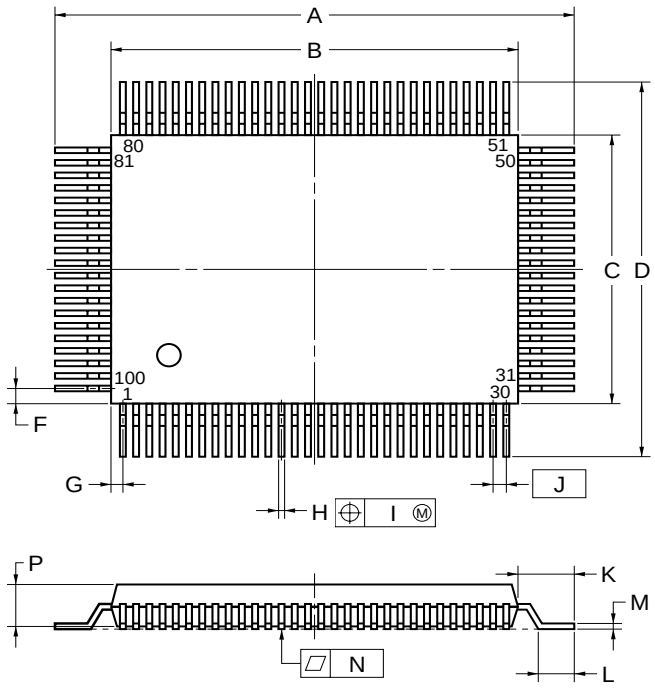


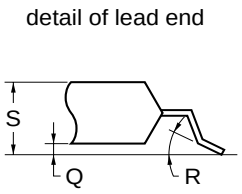

PWBLK
BLK
50 %
50 %
VDD1
VSS1
tPHL3
tPLH3
On
90 %
10 %
VOH2
VOL2
PWPC
PC
50 %
50 %
VDD1
VSS1
tPHL4
tPLH4
On
90 %
10 %
VOH2
VOL2

PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14×20)

100 PIN PLASTIC QFP (14×20)





NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

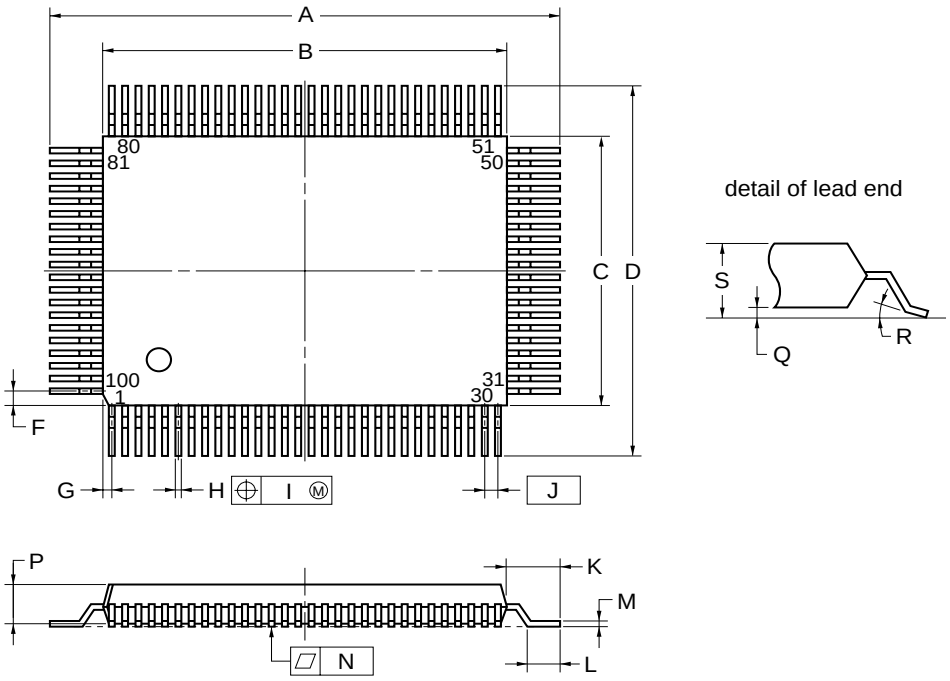
ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA-3

PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14×20)

100 PIN PLASTIC QFP (14×20)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	$0.913^{+0.009}_{-0.008}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.2	0.677±0.008
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S100GF-65-3BA-3

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

SURFACE MOUNT TYPE

For details of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

μPD16327GF-3BA

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230 °C, Duration: 30 sec. MAX. (at 210 °C or above), Number of times: Once, Time limit: None[Note]	IR30-00-1
VPS	Package peak temperature: 215 °C, Duration: 40 sec. MAX. (at 200 °C or above), Number of times: Once, Time limit: None[Note]	VP15-00-1
Pin partial heating	Pin partial temperature: 300 °C MAX., Duration: 10 sec. MAX., Time limit: None[Note]	

Note For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65 % RH.

Caution Use of more than one soldering method should be avoided (except in the case of pin partial heating).

REFERENCES

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)
Quality Grades on NEC Semiconductor Devices (C11531E)

[MEMO]

[MEMO]

M4 96.5