

1/65 DUTY LCD CONTROLLER/DRIVER WITH ON-CHIP RAM

DESCRIPTION

The μ PD16682 is a LCD controller/driver that includes enough RAM capacity to drive full-dot LCD. Each chip can drive a full-dot LCD consisting of up to 132 x 65 dots.

This chip is suitable for cellular phones, Japanese or Chinese-language pagers, and other devices that display Japanese or Chinese characters using either 16 x 16 or 12 x 12 dots per character.

FEATURES

- LCD controller/driver with on-chip display RAM
- Able to operate using +3-V single power supply
- On-chip booster circuit: switchable between 3x and 4x modes
- RAM for dot displays: 132 x 65 bits
- Outputs : 132 segments, 65 commons
- Serial or 8-bit parallel data inputs (switchable between 80 series and 68 series MPUs)
- On-chip divider resistor
- Selectable bias settings (can be set as 1/9 bias or 1/7 bias)
- On-chip oscillation circuit

ORDERING INFORMATION

Part number	Package
μ PD16682W-xxx ^{Note}	Wafer
μ PD16682P-xxx ^{Note}	Chip
μ PD16682N-xxx ^{Note} -051	Standard TCP (output OLB: 0.15-mm pitch), for evaluation

Note The following four temperature gradients can be selected.

-001: -0.05 % / °C

-002: -0.1 % / °C

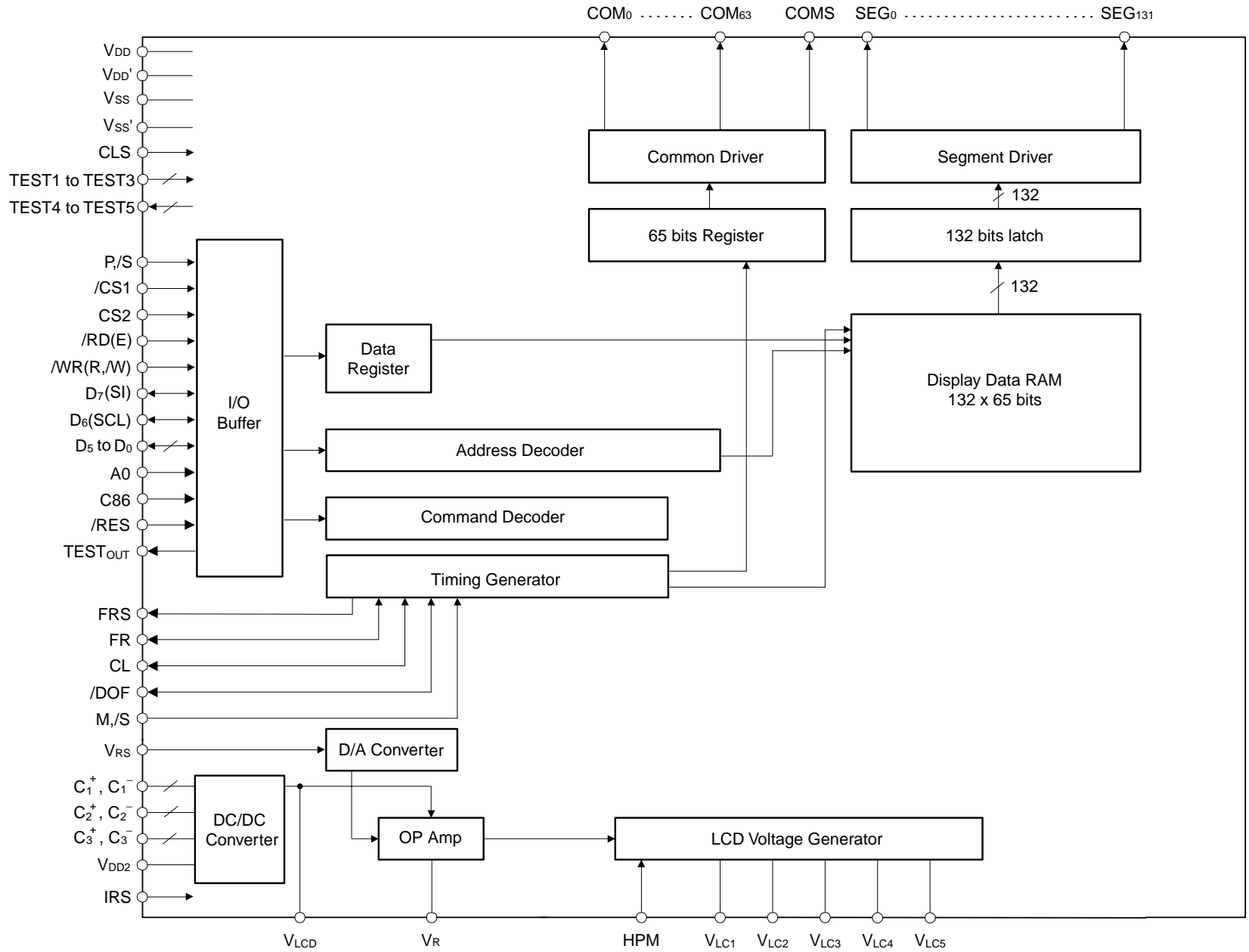
-003: -0.15 % / °C

-004: 0 % / °C

Remark Purchasing the above chip/wafer entails exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representative.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM



Remark /xxx indicates active low signals.

2. PIN CONFIGURATION (Pad Layout)

Chip Size: 2.66 mm x 9.84 mm

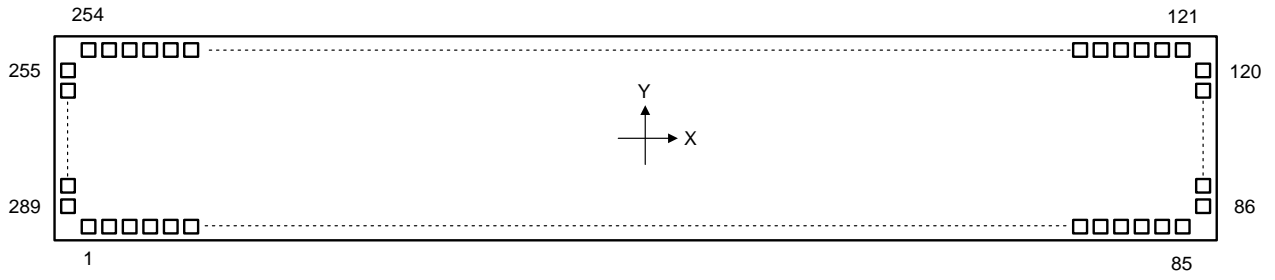


Table 2-1. Pad Layout (1/3)

Pad No.	Pad Name	X [μ m]	Y [μ m]	Pad Type	Pad No.	Pad Name	X [μ m]	Y [μ m]	Pad Type
1	DUMMY1	-3804	-1198	C	59	V _{LC2}	1448	-1198	B
2	FRS	-3682	-1198	B	60	V _{LC2}	1538	-1198	B
3	FR	-3592	-1198	B	61	V _{LC3}	1628	-1198	B
4	CL	-3502	-1198	B	62	V _{LC3}	1718	-1198	B
5	/DOF	-3412	-1198	B	63	V _{LC4}	1808	-1198	B
6	TEST _{OUT}	-3322	-1198	B	64	V _{LC4}	1898	-1198	B
7	V _{SS} '	-3232	-1198	B	65	V _{LC5}	1988	-1198	B
8	/CS1	-3142	-1198	B	66	V _{LC5}	2078	-1198	B
9	CS2	-3052	-1198	B	67	V _{SS} '	2168	-1198	B
10	V _{DD} '	-2962	-1198	B	68	V _{SS} '	2258	-1198	B
11	/RES	-2872	-1198	B	69	TEST1	2348	-1198	B
12	A0	-2782	-1198	B	70	TEST2	2438	-1198	B
13	V _{SS} '	-2692	-1198	B	71	TEST3	2528	-1198	B
14	/WR(R,W)	-2602	-1198	B	72	TEST4	2618	-1198	B
15	/RD(E)	-2512	-1198	B	73	TEST5	2708	-1198	B
16	V _{DD} '	-2422	-1198	B	74	V _{DD} '	2798	-1198	B
17	D ₀	-2332	-1198	B	75	M _{/S}	2888	-1198	B
18	D ₁	-2242	-1198	B	76	CLS	2978	-1198	B
19	D ₂	-2152	-1198	B	77	V _{SS} '	3068	-1198	B
20	D ₃	-2062	-1198	B	78	C86	3158	-1198	B
21	D ₄	-1972	-1198	B	79	P _{/S}	3248	-1198	B
22	D ₅	-1882	-1198	B	80	V _{DD} '	3338	-1198	B
23	D ₆ (SCL)	-1792	-1198	B	81	HPM	3428	-1198	B
24	D ₇ (SI)	-1702	-1198	B	82	V _{SS} '	3518	-1198	B
25	V _{DD}	-1612	-1198	B	83	IRS	3608	-1198	B
26	V _{DD}	-1522	-1198	B	84	V _{DD} '	3698	-1198	B
27	V _{DD}	-1432	-1198	B	85	DUMMY2	3820	-1198	C
28	V _{DD2}	-1342	-1198	B	86	DUMMY3	4788	-1032	C
29	V _{DD2}	-1252	-1198	B	87	COM ₃₁	4788	-940	A
30	V _{DD2}	-1162	-1198	B	88	COM ₃₀	4788	-880	A
31	V _{DD2}	-1072	-1198	B	89	COM ₂₉	4788	-820	A
32	V _{LCD}	-982	-1198	B	90	COM ₂₈	4788	-760	A
33	V _{LCD}	-892	-1198	B	91	COM ₂₇	4788	-700	A
34	V _{LCD}	-802	-1198	B	92	COM ₂₆	4788	-640	A
35	V _{SS}	-712	-1198	B	93	COM ₂₅	4788	-580	A
36	V _{SS}	-622	-1198	B	94	COM ₂₄	4788	-520	A
37	V _{SS}	-532	-1198	B	95	COM ₂₃	4788	-460	A
38	C ₁ ⁺	-442	-1198	B	96	COM ₂₂	4788	-400	A
39	C ₁ ⁺	-352	-1198	B	97	COM ₂₁	4788	-340	A
40	C ₁ ⁻	-262	-1198	B	98	COM ₂₀	4788	-280	A
41	C ₁ ⁻	-172	-1198	B	99	COM ₁₉	4788	-220	A
42	C ₂ ⁺	-82	-1198	B	100	COM ₁₈	4788	-160	A
43	C ₂ ⁺	8	-1198	B	101	COM ₁₇	4788	-100	A
44	C ₂ ⁻	98	-1198	B	102	COM ₁₆	4788	-40	A
45	C ₂ ⁻	188	-1198	B	103	COM ₁₅	4788	20	A
46	C ₃ ⁺	278	-1198	B	104	COM ₁₄	4788	80	A
47	C ₃ ⁺	368	-1198	B	105	COM ₁₃	4788	140	A
48	C ₃ ⁻	458	-1198	B	106	COM ₁₂	4788	200	A
49	C ₃ ⁻	548	-1198	B	107	COM ₁₁	4788	260	A
50	V _{SS} '	638	-1198	B	108	COM ₁₀	4788	320	A
51	V _{DD} '	728	-1198	B	109	COM ₉	4788	380	A
52	V _{DD} '	818	-1198	B	110	COM ₈	4788	440	A
53	V _{RS}	908	-1198	B	111	COM ₇	4788	500	A
54	V _{RS}	998	-1198	B	112	COM ₆	4788	560	A
55	V _R	1088	-1198	B	113	COM ₅	4788	620	A
56	V _R	1178	-1198	B	114	COM ₄	4788	680	A
57	V _{LC1}	1268	-1198	B	115	COM ₃	4788	740	A
58	V _{LC1}	1358	-1198	B	116	COM ₂	4788	800	A

Table 2-1. Pad Layout (2/3)

Pad No.	Pad Name	X [μ m]	Y [μ m]	Pad Type	Pad No.	Pad Name	X [μ m]	Y [μ m]	Pad Type
117	COM ₁	4788	860	A	175	SEG ₅₃	750	1198	A
118	COM ₀	4788	920	A	176	SEG ₅₄	690	1198	A
119	COMS	4788	980	A	177	SEG ₅₅	630	1198	A
120	DUMMY4	4788	1073	C	178	SEG ₅₆	570	1198	A
121	DUMMY5	4023	1198	C	179	SEG ₅₇	510	1198	A
122	SEG ₀	3930	1198	A	180	SEG ₅₈	450	1198	A
123	SEG ₁	3870	1198	A	181	SEG ₅₉	390	1198	A
124	SEG ₂	3810	1198	A	182	SEG ₆₀	330	1198	A
125	SEG ₃	3750	1198	A	183	SEG ₆₁	270	1198	A
126	SEG ₄	3690	1198	A	184	SEG ₆₂	210	1198	A
127	SEG ₅	3630	1198	A	185	SEG ₆₃	150	1198	A
128	SEG ₆	3570	1198	A	186	SEG ₆₄	90	1198	A
129	SEG ₇	3510	1198	A	187	SEG ₆₅	30	1198	A
130	SEG ₈	3450	1198	A	188	SEG ₆₆	-30	1198	A
131	SEG ₉	3390	1198	A	189	SEG ₆₇	-90	1198	A
132	SEG ₁₀	3330	1198	A	190	SEG ₆₈	-150	1198	A
133	SEG ₁₁	3270	1198	A	191	SEG ₆₉	-210	1198	A
134	SEG ₁₂	3210	1198	A	192	SEG ₇₀	-270	1198	A
135	SEG ₁₃	3150	1198	A	193	SEG ₇₁	-330	1198	A
136	SEG ₁₄	3090	1198	A	194	SEG ₇₂	-390	1198	A
137	SEG ₁₅	3030	1198	A	195	SEG ₇₃	-450	1198	A
138	SEG ₁₆	2970	1198	A	196	SEG ₇₄	-510	1198	A
139	SEG ₁₇	2910	1198	A	197	SEG ₇₅	-570	1198	A
140	SEG ₁₈	2850	1198	A	198	SEG ₇₆	-630	1198	A
141	SEG ₁₉	2790	1198	A	199	SEG ₇₇	-690	1198	A
142	SEG ₂₀	2730	1198	A	200	SEG ₇₈	-750	1198	A
143	SEG ₂₁	2670	1198	A	201	SEG ₇₉	-810	1198	A
144	SEG ₂₂	2610	1198	A	202	SEG ₈₀	-870	1198	A
145	SEG ₂₃	2550	1198	A	203	SEG ₈₁	-930	1198	A
146	SEG ₂₄	2490	1198	A	204	SEG ₈₂	-990	1198	A
147	SEG ₂₅	2430	1198	A	205	SEG ₈₃	-1050	1198	A
148	SEG ₂₆	2370	1198	A	206	SEG ₈₄	-1110	1198	A
149	SEG ₂₇	2310	1198	A	207	SEG ₈₅	-1170	1198	A
150	SEG ₂₈	2250	1198	A	208	SEG ₈₆	-1230	1198	A
151	SEG ₂₉	2190	1198	A	209	SEG ₈₇	-1290	1198	A
152	SEG ₃₀	2130	1198	A	210	SEG ₈₈	-1350	1198	A
153	SEG ₃₁	2070	1198	A	211	SEG ₈₉	-1410	1198	A
154	SEG ₃₂	2010	1198	A	212	SEG ₉₀	-1470	1198	A
155	SEG ₃₃	1950	1198	A	213	SEG ₉₁	-1530	1198	A
156	SEG ₃₄	1890	1198	A	214	SEG ₉₂	-1590	1198	A
157	SEG ₃₅	1830	1198	A	215	SEG ₉₃	-1650	1198	A
158	SEG ₃₆	1770	1198	A	216	SEG ₉₄	-1710	1198	A
159	SEG ₃₇	1710	1198	A	217	SEG ₉₅	-1770	1198	A
160	SEG ₃₈	1650	1198	A	218	SEG ₉₆	-1830	1198	A
161	SEG ₃₉	1590	1198	A	219	SEG ₉₇	-1890	1198	A
162	SEG ₄₀	1530	1198	A	220	SEG ₉₈	-1950	1198	A
163	SEG ₄₁	1470	1198	A	221	SEG ₉₉	-2010	1198	A
164	SEG ₄₂	1410	1198	A	222	SEG ₁₀₀	-2070	1198	A
165	SEG ₄₃	1350	1198	A	223	SEG ₁₀₁	-2130	1198	A
166	SEG ₄₄	1290	1198	A	224	SEG ₁₀₂	-2190	1198	A
167	SEG ₄₅	1230	1198	A	225	SEG ₁₀₃	-2250	1198	A
168	SEG ₄₆	1170	1198	A	226	SEG ₁₀₄	-2310	1198	A
169	SEG ₄₇	1110	1198	A	227	SEG ₁₀₅	-2370	1198	A
170	SEG ₄₈	1050	1198	A	228	SEG ₁₀₆	-2430	1198	A
171	SEG ₄₉	990	1198	A	229	SEG ₁₀₇	-2490	1198	A
172	SEG ₅₀	930	1198	A	230	SEG ₁₀₈	-2550	1198	A
173	SEG ₅₁	870	1198	A	231	SEG ₁₀₉	-2610	1198	A
174	SEG ₅₂	810	1198	A	232	SEG ₁₁₀	-2670	1198	A

Table 2-1. Pad Layout (3/3)

Pad No.	Pad Name	X [μ m]	Y [μ m]	Pad Type
233	SEG ₁₁₁	-2730	1198	A
234	SEG ₁₁₂	-2790	1198	A
235	SEG ₁₁₃	-2850	1198	A
236	SEG ₁₁₄	-2910	1198	A
237	SEG ₁₁₅	-2970	1198	A
238	SEG ₁₁₆	-3030	1198	A
239	SEG ₁₁₇	-3090	1198	A
240	SEG ₁₁₈	-3150	1198	A
241	SEG ₁₁₉	-3210	1198	A
242	SEG ₁₂₀	-3270	1198	A
243	SEG ₁₂₁	-3330	1198	A
244	SEG ₁₂₂	-3390	1198	A
245	SEG ₁₂₃	-3450	1198	A
246	SEG ₁₂₄	-3510	1198	A
247	SEG ₁₂₅	-3570	1198	A
248	SEG ₁₂₆	-3630	1198	A
249	SEG ₁₂₇	-3690	1198	A
250	SEG ₁₂₈	-3750	1198	A
251	SEG ₁₂₉	-3810	1198	A
252	SEG ₁₃₀	-3870	1198	A
253	SEG ₁₃₁	-3930	1198	A
254	DUMMY6	-4022	1198	C
255	DUMMY7	-4788	1032	C
256	COM ₃₂	-4788	940	A
257	COM ₃₃	-4788	880	A
258	COM ₃₄	-4788	820	A
259	COM ₃₅	-4788	760	A
260	COM ₃₆	-4788	700	A
261	COM ₃₇	-4788	640	A
262	COM ₃₈	-4788	580	A
263	COM ₃₉	-4788	520	A
264	COM ₄₀	-4788	460	A
265	COM ₄₁	-4788	400	A
266	COM ₄₂	-4788	340	A
267	COM ₄₃	-4788	280	A
268	COM ₄₄	-4788	220	A
269	COM ₄₅	-4788	160	A
270	COM ₄₆	-4788	100	A
271	COM ₄₇	-4788	40	A
272	COM ₄₈	-4788	-20	A
273	COM ₄₉	-4788	-80	A
274	COM ₅₀	-4788	-140	A
275	COM ₅₁	-4788	-200	A
276	COM ₅₂	-4788	-260	A
277	COM ₅₃	-4788	-320	A
278	COM ₅₄	-4788	-380	A
279	COM ₅₅	-4788	-440	A
280	COM ₅₆	-4788	-500	A
281	COM ₅₇	-4788	-560	A
282	COM ₅₈	-4788	-620	A
283	COM ₅₉	-4788	-680	A
284	COM ₆₀	-4788	-740	A
285	COM ₆₁	-4788	-800	A
286	COM ₆₂	-4788	-860	A
287	COM ₆₃	-4788	-920	A
288	COMS	-4788	-980	A
289	DUMMY8	-4788	-1073	C

Remark Pad Type A:
 Pad size(AI): 47 x 105 μ m²(TYP.)
 Bump size: 35 x 92.5 μ m²(TYP.)
 Bump height: 17 μ m(TYP.)
 Pad Type B:
 Pad size(AI): 75 x 105 μ m²(TYP.)
 Bump size: 67 x 92.5 μ m²(TYP.)
 Bump height: 17 μ m(TYP.)
 Pad Type C:
 Pad size(AI): 118 x 105 μ m²(TYP.)
 Bump size: 110 x 92.5 μ m²(TYP.)
 Bump height: 17 μ m(TYP.)

3. PIN DESCRIPTIONS

3.1 Power Supply System Pins

Pin Symbol	Pin Name	Pad No.	I/O	Function Description
V _{DD}	Logic power supply pins	25 to 27	—	Power supply pins for logic. Apply the logic power supply voltage from an external source.
V _{DD2}	Booster circuit power supply pins	28 to 31	—	Power supply pins for booster circuit. Apply the booster circuit power supply voltage from an external source.
V _{SS}	Logic/driver ground pins	35 to 37	—	Ground pins for logic and driver circuit. Connect these pins to an external ground.
V _{LCD}	Driver power supply pins	32 to 34	—	Power supply pins for driver. Output pins for internal booster circuit. Connect a 1- μ F capacitor for boosting between these pins and the GND pins. If not using the internal booster circuit, a direct driver power supply can be input.
V _{DD} '	Power supply pins for fixed mode pins	10,16,51, 52,74,80, 84	—	These power supply pins are used to set the mode pins as fixed.
V _{SS} '	Ground pins for fixed mode pins	7,13,50, 67,68,77, 82	—	These ground pins are used to set the mode pins as fixed.
V _{LC1} to V _{LC5}	Reference power supply pins for driver	57 to 66	—	These are reference power supply pins for the LCD driver. Connect a smoothing capacitor if an internal bias has been selected.
C ₁ ⁺ , C ₁ ⁻ C ₂ ⁺ , C ₂ ⁻ C ₃ ⁺ , C ₃ ⁻	Capacitor connection pins	38 to 49	—	These are capacitor connection pins for the booster circuit. Connect a 1- μ F capacitor.

3.2 Logic System Pins (1/2)

Pin Symbol	Pin Name	Pad No.	I/O	Function Description
P ₀ /S	Select data input	79	Input	This pin is used to select between parallel data input and serial data input. P ₀ /S = H : Parallel data input P ₀ /S = L : Serial data input This setting cannot be switched after power-on. For details, see 5. DESCRIPTION OF FUNCTIONS.
/CS1,CS2	Chip select	8,9	Input	These pins are used for the chip select signal. When /CS1 = L and CS2 = H, this signal is active and can be used for I/O of data and commands.
/RD(E)	Read (enable)	15	Input	<ul style="list-style-type: none"> When connected to 80 series MPU : active low This pin connects the 80 series MPU's RD signal. Data bus output status is set when this signal is low. <ul style="list-style-type: none"> When connected to 68 series MPU : active high It is used as the enable clock input pin for the 68 series MPU.
/WR(R, ₀ W)	Write (read/write)	14	Input	<ul style="list-style-type: none"> When connected to 80 series MPU: active low This pin connects the 80 series MPU's /WR signal. Signals on the data bus are latched at the rising edge of the /WR signal. <ul style="list-style-type: none"> When connected to 68 series MPU This pin is an input pin for read/write control signals. R ₀ /W = H : Read R ₀ /W = L : Write
C86	Interface select	78	Input	This pin is used to select the MPU interface. C86 = H : 68 series MPU interface C86 = L : 80 series MPU interface
D ₀ to D ₅	Data bus	17 to 22	Input /Output	When used with a parallel interface, these pins correspond to data bus bits D ₀ to D ₅ . When used with a serial interface, they are pulled down internally.
D ₆ (SCL)	Data bus/serial clock	23	Input /Output	When used with a parallel interface, this pin corresponds to data bus bit D ₆ . When used with a serial interface, it is a serial clock input pin.
D ₇ (SI)	Data bus/serial data input	24	Input /Output	When used with a parallel interface, this pin corresponds to data bus bit D ₇ . When used with a serial interface, it is a serial data input pin.
A0	Data command	12	Input	This pin is connected to the LSB in the ordinary MPU address bus to distinguish between data and commands. A0 = H : Indicates that display data exists in bits D ₀ to D ₇ . A0 = L : Indicates that display control commands exist in bits D ₀ to D ₇ .
TEST _{OUT}	Test output	6	Output	This pin is used as a test output. Leave this pin open when used for this purpose.
/RES	Reset	11	Input	This pin is used to perform an internal reset when at low level.
CLK	Clock select	76	Input	This pin is used to select the valid/invalid setting for the display clock's on-chip oscillation circuit. CLS = H : On-chip oscillation circuit is valid CLS = L : On-chip oscillation circuit is invalid (external input) When CLS = L, a display clock is input via the CL pin.

3.2 Logic System Pins (2/2)

Pin Symbol	Pin Name	Pad No.	I/O	Function Description																																						
FR	Frame signal	3	Input /Output	This pin is used as an I/O pin for the LCD's AC conversion signal. This pin is used (along with the FRS pin) for the static drive.																																						
FRS	Static signal	2	Output	This pin is used as an output pin for the static drive. This pin is used (along with the FR pin) for the static drive.																																						
M,/S	Master/Slave	75	Input	This pin is used to select master or slave operation mode. Timing signals required for the LCD are output during master mode and are input during slave mode to ensure synchronization of the LCD block. M,/S = H: Master operation mode M,/S = L: Slave operation mode Note the settings below, based on the status of the M,/S and CLS pins. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>M,/S</th> <th>CLS</th> <th>Oscillation Circuit</th> <th>Power supply circuit</th> <th>CL</th> <th>FR</th> <th>FRS</th> <th>/DOF</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>Valid</td> <td>Valid</td> <td>Output</td> <td>Output</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Invalid</td> <td>Valid</td> <td>Input</td> <td>Output</td> <td>Output</td> <td>Output</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>Invalid</td> <td>Invalid</td> <td>Input</td> <td>Input</td> <td>Hi-Z</td> <td>Input</td> </tr> <tr> <td>L</td> <td>Invalid</td> <td>Invalid</td> <td>Input</td> <td>Input</td> <td>Hi-Z</td> <td>Input</td> </tr> </tbody> </table>	M,/S	CLS	Oscillation Circuit	Power supply circuit	CL	FR	FRS	/DOF	H	H	Valid	Valid	Output	Output	Output	Output	L	Invalid	Valid	Input	Output	Output	Output	L	H	Invalid	Invalid	Input	Input	Hi-Z	Input	L	Invalid	Invalid	Input	Input	Hi-Z	Input
M,/S	CLS	Oscillation Circuit	Power supply circuit	CL	FR	FRS	/DOF																																			
H	H	Valid	Valid	Output	Output	Output	Output																																			
	L	Invalid	Valid	Input	Output	Output	Output																																			
L	H	Invalid	Invalid	Input	Input	Hi-Z	Input																																			
	L	Invalid	Invalid	Input	Input	Hi-Z	Input																																			
CL	Display clock input	4	Input /Output	This pin is used as the display clock I/O pin. Note the settings below, based on the status of the M,/S and CLS pins. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>M,/S</th> <th>CLS</th> <th>CL</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Input</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>Input</td> </tr> <tr> <td>L</td> <td>Input</td> </tr> </tbody> </table> When using this pin in master or slave mode, connect it to the corresponding CL pin.	M,/S	CLS	CL	H	H	Output	L	Input	L	H	Input	L	Input																									
M,/S	CLS	CL																																								
H	H	Output																																								
	L	Input																																								
L	H	Input																																								
	L	Input																																								
/DOF	Blink control	5	Input /Output	This pin is used to control blinking in the LCD. M,/S = H : Output M,/S = L : Input When using this pin in master or slave mode, connect it to the corresponding /DOF pin.																																						
HPM	Power supply circuit select pin for LCD driver	81	Input	This pin is used as a power control pin of the power supply circuit for the LCD driver. HPM = H : Normal mode HPM = L : High-power mode																																						
IRS	Select pin for V _{LC1} regulating resistor	83	Input	This pin is used to select the resistor that is used to regulate the V _{LC1} voltage. IRS = H : Select on-chip resistor IRS = L : Do not select on-chip resistor. The V _{LC1} voltage is regulated via the V _R pin and an external divided resistor. Use of the on-chip resistor cannot be selected or deselected via a hard reset or via a reset command. Instead, use this pin to select the setting.																																						
TEST1 to TEST3	Test pins	69 to 71	Input	These are test pins for IC tests. Normally, these pins should be left open.																																						
TEST4,TEST5	Test pins	72,73	Output	These are test pins for IC tests. Normally, these pins should be left open.																																						

3.3 Driver System Pins

Pin Symbol	Pin Name	Pad No.	I/O	Function Description
SEG ₀ to SEG ₁₃₁	Segment	122 to 253	Output	Segment output pins
COM ₀ to COM ₆₃	Common	87 to 118, 256 to 287	Output	Common output pins
COMS	Indicator common	288	Output	Common output pins for indicator The same signal is output from pin 2.
V _{RS}	Op amp inputs	53,54	Input	These are input pins for the op amp that regulates the LCD driver voltage. Leave the V _{RS} pin open when using the on-chip power supply. When not using the on-chip power supply, a reference voltage V _{REG} must be input. When using an external power supply, connect the V _R pin to a resistor used to regulate the LCD voltage.
V _R		55,56		
DUMMY1 to DUMMY5	Dummy pins	1,85,86, 120,121	—	Since these pins are not connected to any internal circuits, they should be left open when they are not being used.

4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in the following table.

Pin Name	I/O	Recommended Connection of Unused Pins	Notes
P ₀ /S	Input	Mode setting pin	1
/CS1	Input	Connect to V _{SS}	
CS2	Input	Connect to V _{DD}	
/RD(E)	Input	Connect to V _{DD} (80 series interface), connect to V _{DD} or V _{SS} (serial interface)	
/WR (R,/W)	Input	Connect to V _{DD} or V _{SS} (serial interface)	
C86	Input	Mode setting pin	1
D ₀ to D ₅	Input/Output	Leave open (when using serial interface)	4
D ₆ (SCL)	Input/Output		
D ₇ (SI)	Input/Output		
A0	Input	Data/command setting pin	2
TEST _{OUT}	Output	Leave open	
/RES	Input	Connect to V _{DD}	
CLS	Input	Mode setting pin	1
FR	Input/Output	Leave open (when using master mode, M,/S = H)	
FRS	Output	Leave open	
/DOF	Input/Output	Leave open (when using master mode, M,/S = H)	
M,/S	Input	Mode setting pin	1
CL	Input/Output	Display clock	3
HPM	Input	Mode setting pin	1
IRS	Input	Mode setting pin	1
TEST1	Input	Leave open	4
TEST2	Input	Leave open	4
TEST3	Input	Leave open	4
TEST4	Output	Leave open	
TEST5	Output	Leave open	

- Notes**
1. Connect to V_{DD} or V_{SS} according to the selected mode.
 2. Input microcontroller output from V_{DD} or V_{SS} according to the selected register.
 3. This pin is an output when M,/S = H and CLS = H but should otherwise be used to input the display clock.
 4. These pins are pulled down to V_{SS} in the IC.

5. DESCRIPTION OF FUNCTIONS

5.1 MPU Interface

5.1.1 Select interface type

The μ PD16682 transfers data either via an 8-bit bidirectional data bus (D₇ to D₀) or via a serial data input (SI). The P₁/S pin can be set to either high or low levels to select 8-bit parallel data input or serial data input, as shown in the table below.

P ₁ /S	/CS1	CS2	A0	/RD	/WR	C86	D ₇	D ₆	D ₅ - D ₀
H: Parallel input	/CS1	CS2	A0	/RD	/WR	C86	D ₇	D ₆	D ₅ -D ₀
L: Serial input	/CS1	CS2	A0	Note 1	Note 1	Note1	SI	SCL	Note2

Notes 1. Fix this pin as either H or L.

2. High impedance

5.1.2 Parallel interface

If the parallel interface has been selected (P₁/S = H), setting the C86 pin either high or low determines whether to connect directly to the 80 series MPU or the 68 series MPU, as shown in the table below.

P ₁ /S	/CS1	CS2	A0	/RD	D ₇ - D ₀
H: 68 series MPU bus	/CS1	CS2	A0	E	D ₇ - D ₀
L: 80 series MPU bus	/CS1	CS2	A0	/RD	D ₇ - D ₀

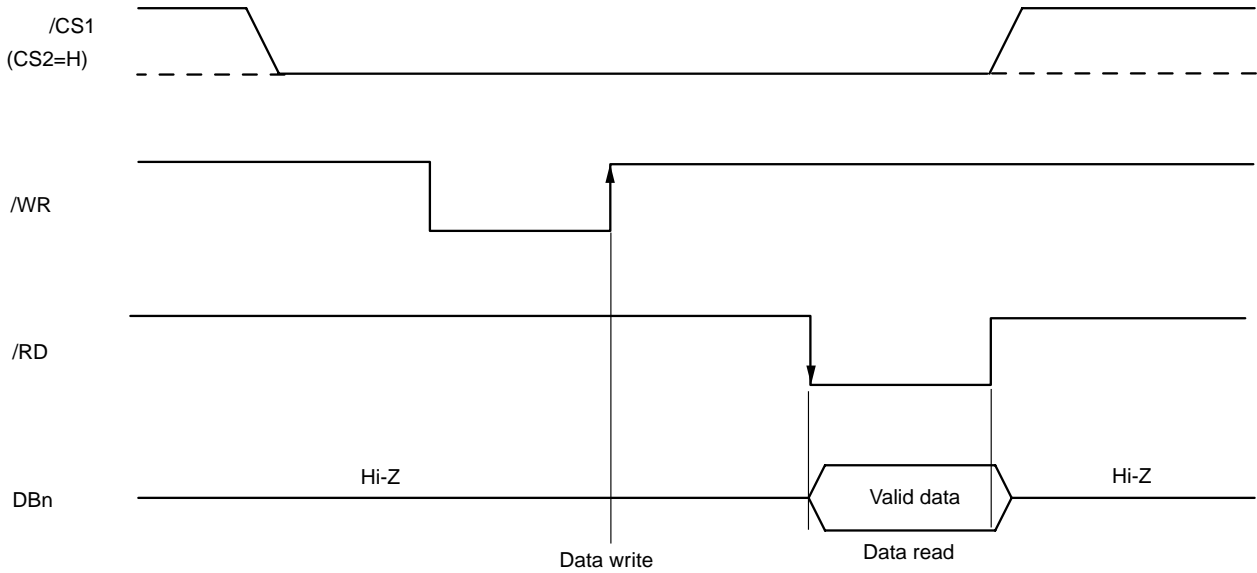
The data bus signal can be identified according to the combination of A0, /RD(E), and /WR (R,/W) signals, as shown in the table below.

Common	68 Series	80 Series		Function
	R,/W	/RD	/WR	
H	H	L	H	Read display data
H	L	H	L	Write display data
L	H	L	H	Read status
L	L	H	L	Write control data (command)

(1) 80 Series Parallel Interface

When 80 series parallel data transfer has been selected, data is written to the μ PD16682 at the rising edge of the /WR signal. The data is output to the data bus when the /RD signal is L.

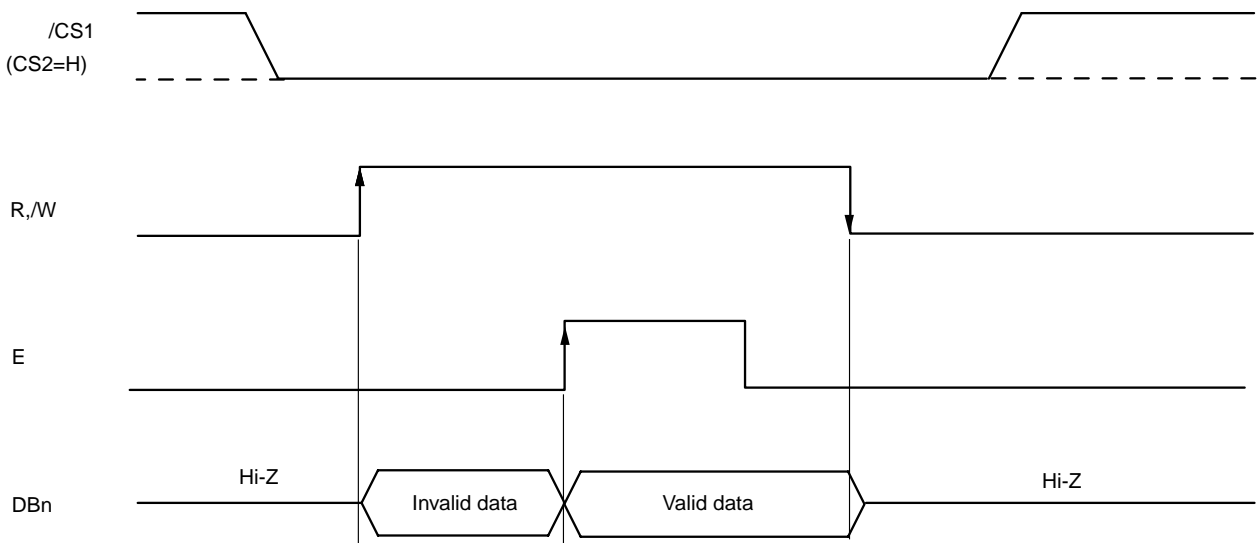
Figure 5-1. 80 Series Interface Data Bus Status



(2) 68 Series Parallel Interface

When 68 series parallel data transfer has been selected, data is written at the falling edge of the E signal when the R,/W signal is L. During the data read operation, the data bus enters the output status when the R,/W signal is H, outputs valid data at the rising edge of the E signal, and enters the high-impedance state at the falling edge of the R,/W signal (R,/W = L).

Figure 5-2. 68 Series Interface Data Bus Status



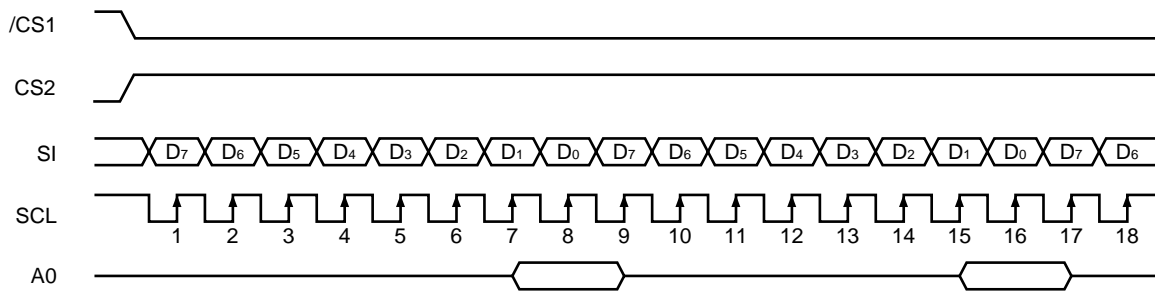
5.1.3 Serial interface

If the serial interface has been selected ($P_{/S} = L$) and if the chip is in the active state ($/CS1 = L$ and $CS2 = H$), both serial data input (SI) and serial clock input (SCL) can be received. The serial interface includes an 8-bit shift register and a 3-bit counter. Serial data is captured at the rising edge of the serial clock and is clocked in via the serial data input pins in sequence from D_7 to D_0 . At the rising edge of the eighth serial clock, data is converted to 8-bit parallel data.

Input via the $A0$ pin can be used to determine whether the input serial data is display data or a command (display data when $A0 = H$, command when $A0 = L$). The timing for reading and identifying input via $A0$ occurs at the rising edge of the “eighth x n” serial clock once the chip’s status is active.

A serial interface signal chart is shown below.

Figure 5–3. Serial Interface chart



- Remarks 1.** When the chip’s status is inactive, the shift register and counter are both reset to their initial values.
2. Data cannot be read when using the serial interface.
 3. For the SCL signal, caution is advised concerning the wire’s terminating reflection and noise from external sources. We recommend to check the operation on the actual equipment.

5.1.4 Chip select

The μ PD16682 has two chip select pins ($/CS1$ and $CS2$). The MPU interface or serial interface can be used only when $/CS1 = L$ and $CS2 = H$.

When the chip select pin is inactive, D_7 to D_0 are set to high impedance (invalid) and input of $A0$, $/RD$, or $/WR$ is invalid. If the serial interface has been selected, the shift register and counter are both reset.

5.1.5 Display data RAM and internal register access

Access to the μ PD16682 from the MPU supports high-speed data transfers since the cycle time (t_{CYC}) is met and there is no need for wait time.

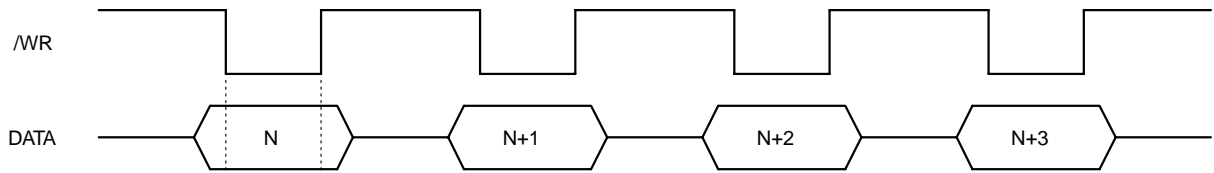
When data transfer occurs between the μ PD16682 and the MPU, the data is held in a bus holder belonging to the internal data bus and is written to the display data RAM before the next data write cycle. When the MPU reads the contents of the display data RAM, the data read during the first data read cycle (dummy cycle) is first held in the bus holder and is read from the bus holder to the system bus during the next data read cycle.

Note with caution that, due to constraints on the read sequence for the display data RAM, when the address is set, the data is not output from the address specified by the next read command but rather is output to the address specified during the second data read operation. Consequently, one dummy read operation is strictly required after setting an address or after a write cycle. Figure 5–4 illustrates this situation.

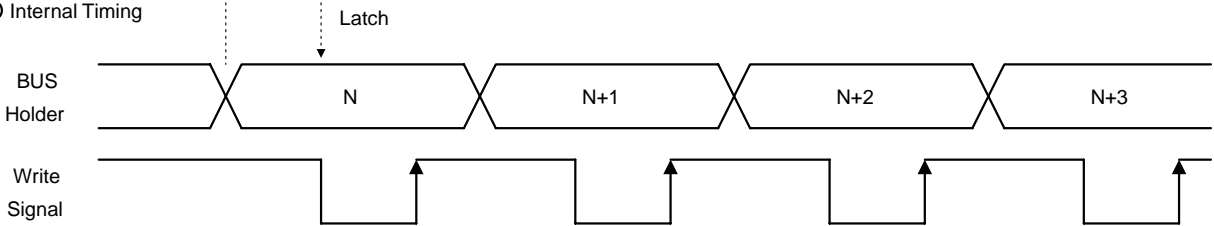
Figure 5-4. Write and Read Operations

Writing

○MPU

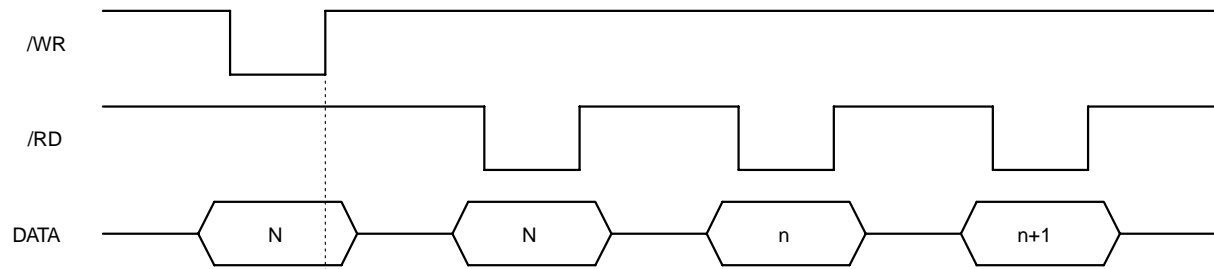


○ Internal Timing

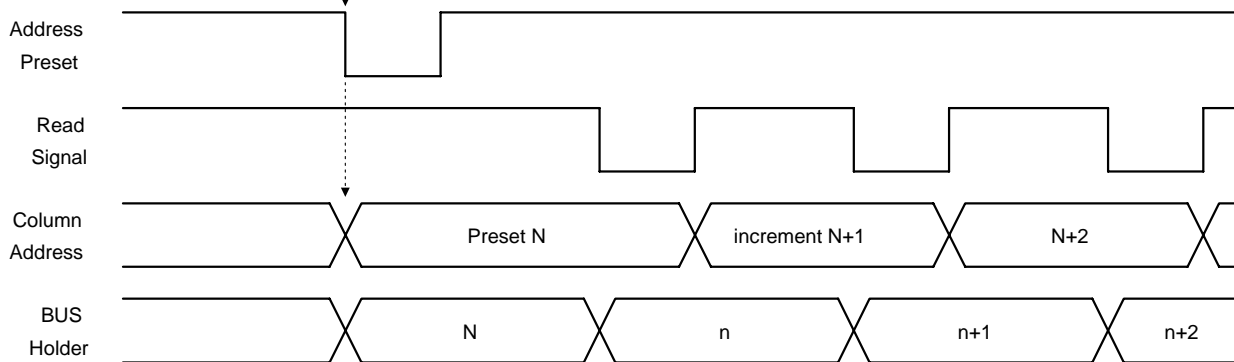


Reading

○MPU



○ Internal Timing



6. DISPLAY DATA RAM

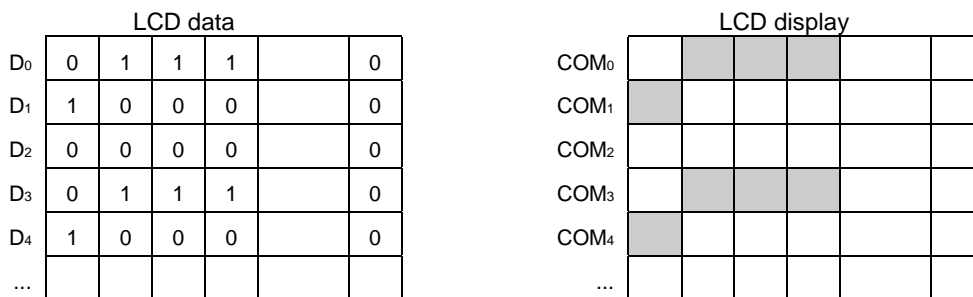
6.1 Display Data RAM

This is the RAM that is used to store the display's dot data. The RAM configuration is 65 (8 pages x 8 bits + 1) x 132 bits. Any specified bit can be accessed by selecting the corresponding page address and column address.

As is shown in Figure 6-1 below, the display data (D₇ to D₀) from the MPU corresponds to the common direction in the LCD, so that if a multiple set of μ PD16682 chips is used, there are fewer constraints on transfers of display data and relatively more freedom for display configurations.

The MPU accesses the display data RAM for read/write operations via the I/O buffer, and these operations are independent of the LCD driver signal read operations. Therefore, there are absolutely no adverse effects (such as flicker) in the display when display data RAM is accessed asynchronously in relation to the LCD contents.

Figure 6-1. LCD Data and LCD Display



6.2 Page Address Circuit

The page address set command specifies the page address in the display data RAM, as is shown in Figure 6-2. To access a different page, simply specify a different page address using this command.

Page address 8 (D₃,D₂,D₁,D₀ = 1,0,0,0) is a RAM area that is used exclusively for indicator, so only display data D₀ is valid.

6.3 Column Address Circuit

The column address set command specifies the column address in the display data RAM, as is shown in Figure 6-2. The specified column address is incremented each time a display data read or write command is input, so the MPU is able to successively access display data.

Incrementation of the column address stops at 83H. The column address and page address are mutually independent, which means that to switch from column 83H on page 0 to column 00H on page 1, both the page address and column address must be separately specified again.

Also, as is shown in Table 6-1, the ADC command (segment driver direction select command) can be used to invert the correspondence between the display data RAM's column address and segment output. This reduces the number of IC layout constraints that are imposed when setting up the LCD module.

Table 6-1. Relation between Display Data RAM Column Address and Segment Output

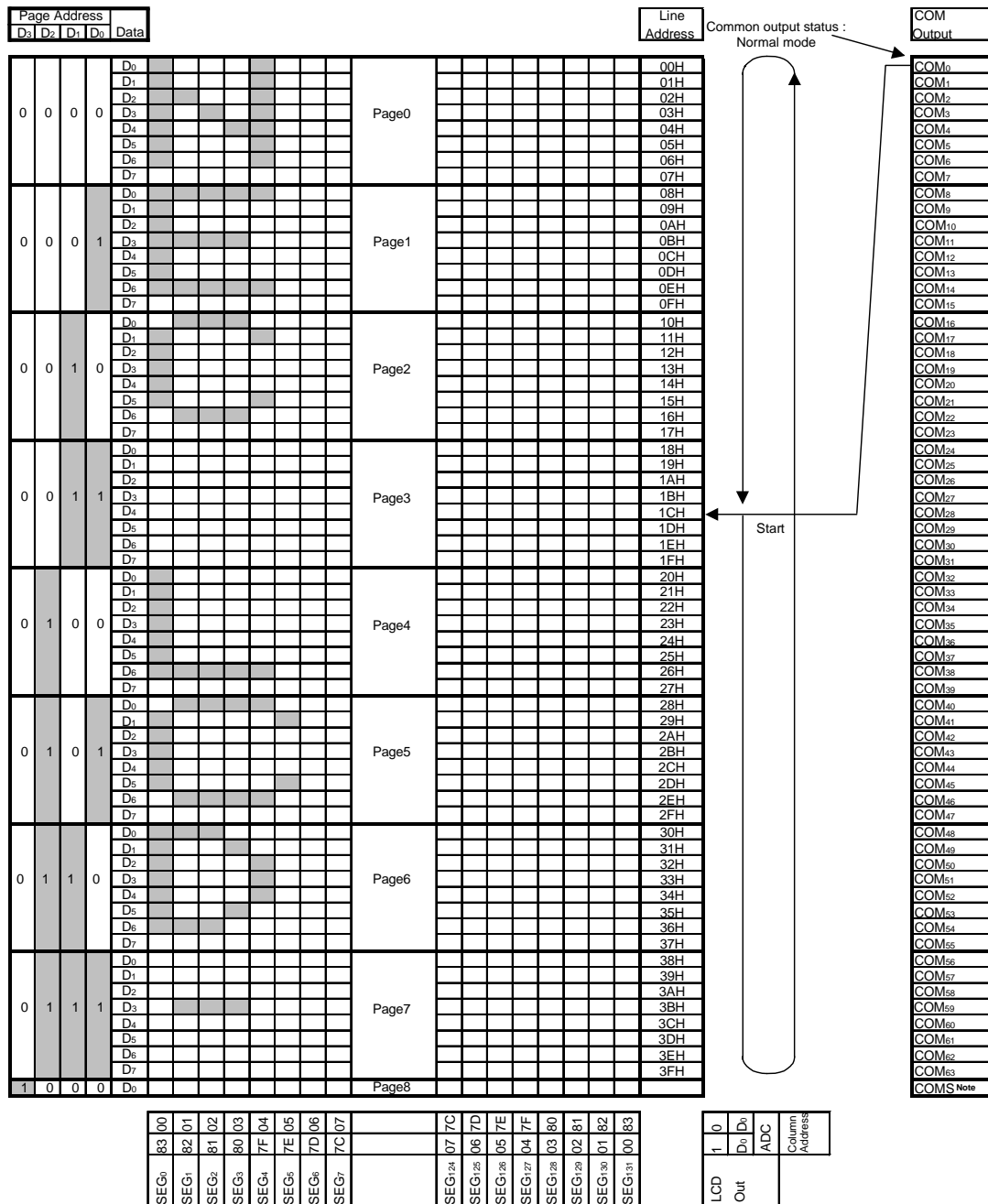
SEG Output		SEG ₀		SEG ₁₃₁
ADC (D ₀)	"0"	00H	→ Column Address →	83H
	"1"	83H	← Column Address ←	00H

6.4 Line Address Circuit

As is shown in Figure 6-2, the line address circuit specifies the line address that corresponds to a COM output for displaying the contents of display data RAM. The display start line address set command usually specifies the highest line in the display (corresponding to the COM₀ output when in normal mode or the COM₆₃ output when in inverted mode). Thus, there are 65 lines in the direction of incrementation of line address starting from the specified display start line address.

The screen can be scrolled by dynamically changing the line address via the display start line address set command.

Figure 6-2. Specification of Display Start Line Address in Display Data RAM



Note COMS accesses the 65th line regardless of the display start line address.

6.5 Display Data Latch Circuit

The display data latch circuit is used for temporary storage of display data that has been output to the LCD driver circuit from the display data RAM.

The commands that are used to set normal/inverted display modes, display ON/OFF status, and display all ON/OFF status are commands that control data in this latch so that there is no modification of the data in the display data RAM.

7. OSCILLATION CIRCUIT

This is a CR-type oscillation circuit that generates the display clock. The oscillation circuit is valid only when CLS = H. When CLS = L, oscillation is stopped and the display clock is input via the CL pin.

8. DISPLAY TIMING GENERATOR

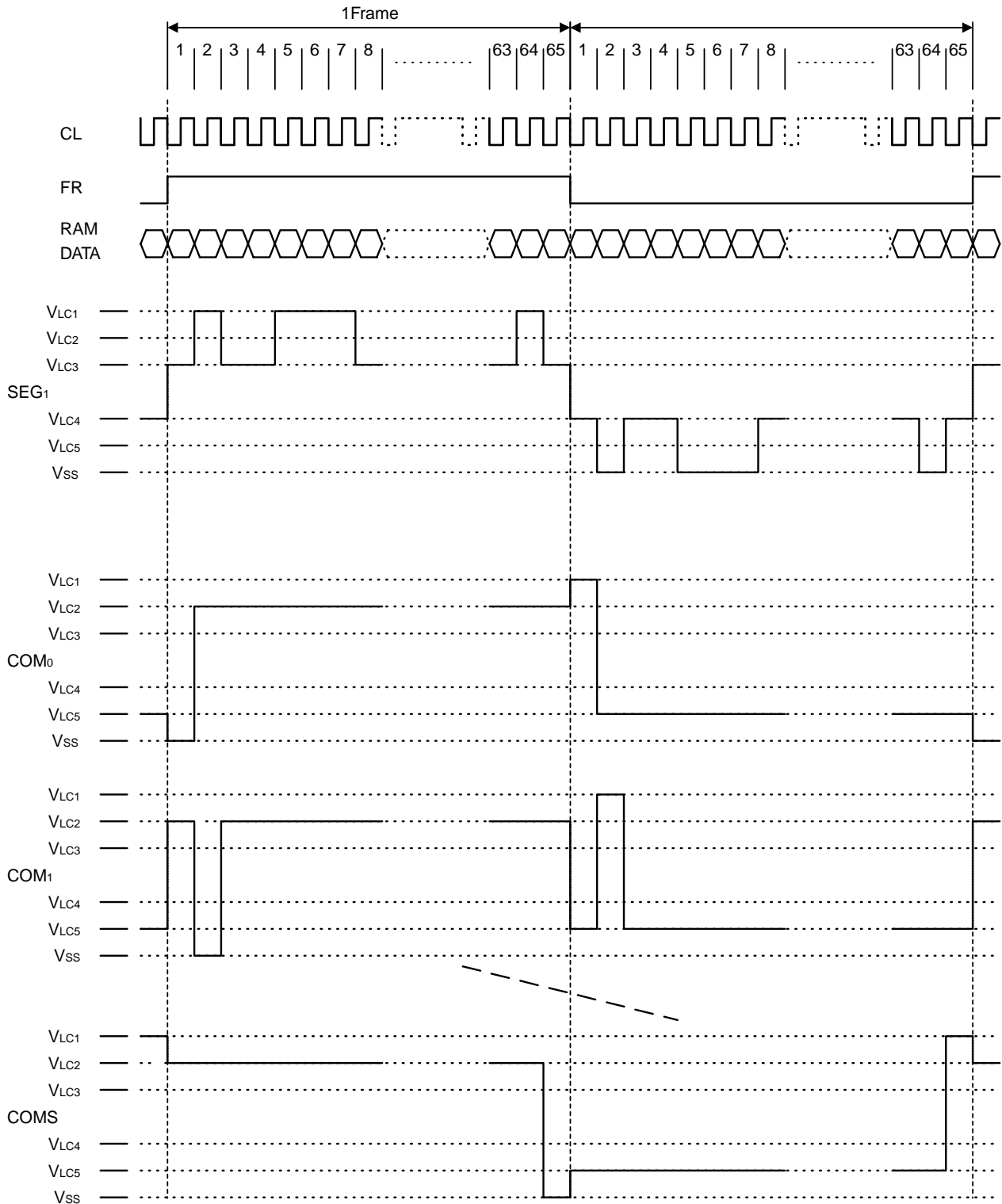
The display timing generator generates timing signals from the display clock to the line address circuit and the display data latch circuit. Display data is latched into the display data latch circuit in synch with the display clock and is output via segment driver output pins. Reading of the display data is completely independent of the MPU's accessing of the display data RAM. Consequently, there are no adverse effects (such as flicker) on the LCD panel even when the display data RAM is accessed asynchronously in relation to the LCD contents.

The internal common timing and LCD's AC conversion signal (FR) are both generated from the display clock. As is shown in Figure 8-1, a drive waveform based on the two-frame AC drive method is generated for the LCD driver circuit.

If a multiple set of μ PD16682 chips is used, the display timing signals (FR, CL, and /DOF) for the slave side must be supplied from the master side.

Operation Mode		FR	CL	/DOF
Master (M,/S = H)	On-chip oscillation circuit is valid (CLS = H)	Output	Output	Output
	On-chip oscillation circuit is invalid (CLS = L)	Output	Input	Output
Slave (M,/S = L)	On-chip oscillation circuit is invalid (CLS = H)	Input	Input	Input
	On-chip oscillation circuit is invalid (CLS = L)	Input	Input	Input

Figure 8-1. Drive Waveform when Using Two-Frame AC Drive Method



9. COMMON OUTPUT STATUS SELECT CIRCUIT

With the μ PD16682, the common output status select command can be used to set the scan direction for COM outputs (see Table 9-1). As a result, there are fewer IC layout constraints when setting up the LCD module.

Table 9-1. Setting of Scan Direction for COM Outputs

Status	COM Scan Direction	
Normal (forward)	COM ₀	→ COM ₆₃
Inverted (reverse)	COM ₆₃	→ COM ₀

10. POWER SUPPLY CIRCUIT

10.1 Power Supply Circuit

The power supply circuit, which supplies the voltage needed to drive the LCD, includes a booster circuit, voltage regulator circuit, and voltage follower circuit.

The power control set command is used to control the ON/OFF status of the power supply circuit's booster circuit, voltage regulator circuit (V regulator circuit), and voltage follower circuit (V/F circuit). This makes it possible to jointly use an external power supply along with certain functions of the on-chip power supply. Table 10-1 shows the function that controls the 3-bit data in the power control set command and Table 10-2 shows a reference chart of combinations.

Table 10-1. Control Values Set to Bits in Power Control Set Command

Item		Status	
		H	L
D ₂	Booster circuit control bit	ON	OFF
D ₁	Voltage regulator circuit control bit	ON	OFF
D ₀	Voltage follower circuit control bit	ON	OFF

Table 10-2. Reference Chart of Combinations

Use Status	D ₂	D ₁	D ₀	Booster Circuit	V Regulator Circuit	V/F Circuit	External Power Supply Input	Booster-related Pin
<1> Use on-chip power supply	H	H	H	○	○	○	V _{DD2}	Used
<2> Use V regulator circuit and V/F circuit only	L	H	H	×	○	○	V _{LCB}	Open
<3> Use V/F circuit only	L	L	H	×	×	○	V _{LC1}	Open
<4> Use External power supply only	L	L	L	×	×	×	V _{LC1} to V _{LC5}	Open

- Remarks**
1. The booster-related pins are indicated as pins C₁⁺, C₁⁻, C₂⁺, C₂⁻, C₃⁺, and C₃⁻.
 2. Although combinations other than those shown above are possible, they have no practical uses and therefore cannot be recommended.

10.2 Booster circuit

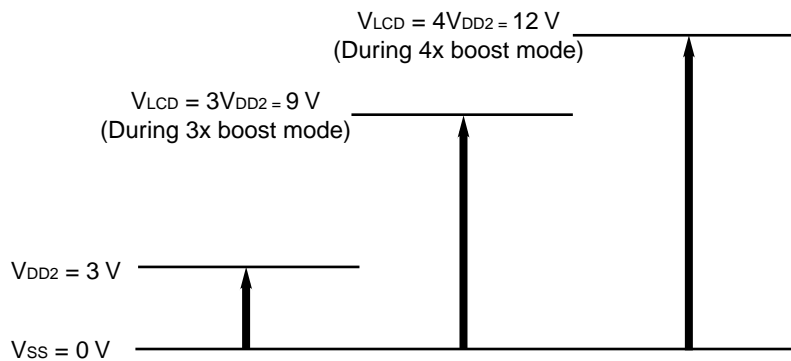
3x and 4x booster circuits have been incorporated in chip to generate the current driving the LCD.

When using the internal power supply, connect the booster-related capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, and $C3^+$ and $C3^-$. Also, connect the level stabilization-related capacitor between V_{LCD} and V_{SS} and set D_2 high to boost the potential between V_{DD2} and V_{SS} from 3 to 4 times.

Since the booster circuit uses signals from the internal oscillation circuit, the oscillation circuit must be operating. The relation between the boosted voltage and the potential is described below.

The $C1^+$, $C1^-$, $C2^+$, $C2^-$, $C3^+$, $C3^-$, and V_{DD2} pins all relate to the booster circuit, so the wire impedance should be minimized.

Figure 10-1. 3x and 4x Booster Circuits



Caution When set to 3x boost mode, connect booster-related capacitors between $C2^-$ and $C3^+$ and between $C1^+$ and $C1^-$.

10.3 Voltage Regulator Circuit

The boost voltage that was generated at V_{LCD} is output via the voltage regulator circuit as the LCD drive voltage V_{LC1} . Since the μ PD16682 has a 64-level electronic volume function and an on-chip resistor for V_{LC1} voltage regulation, various components can be used to configure a highly accurate voltage regulator circuit.

10.3.1 Use of on-chip resistor for V_{LC1} voltage regulation

The on-chip resistor for V_{LC1} voltage regulation and the electronic volume function can be used to regulate the darkness of the LCD contents, not only by adding an external resistor but also by controlling the LCD drive voltage V_{LC1} by using commands only. The V_{LC1} voltage can be determined using equation 10-1 as within the range of $V_{LC1} < V_{LCD}$.

Equation 10-1.

$$V_{LC1} = (1 + \frac{R_b}{R_a})V_{EV}$$

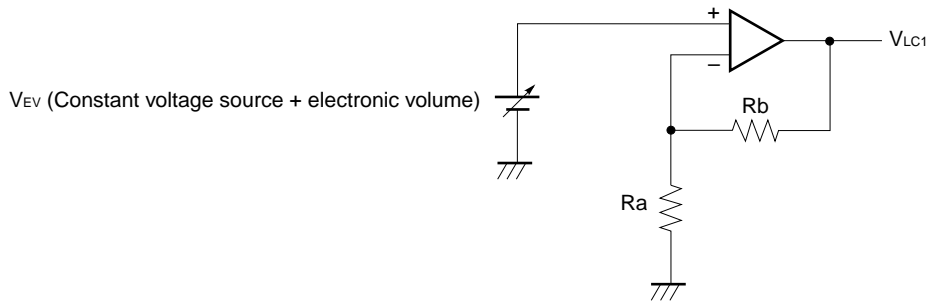
The equation for determining V_{EV} varies according to the product code (temperature gradient).

$$V_{EV} = \frac{162}{203}(1 - \frac{\alpha}{162})V_{REG} \text{ (-001 code, } -0.05\% / ^\circ\text{C)}$$

$$V_{EV} = \frac{162}{178}(1 - \frac{\alpha}{162})V_{REG} \text{ (-002 code, } -0.1\% / ^\circ\text{C)}$$

★ $V_{EV} = (1 - \frac{\alpha}{162})V_{REG} \text{ (-003 code, } -0.15\% / ^\circ\text{C)}$

★ $V_{EV} = \frac{162}{236}(1 - \frac{\alpha}{162})V_{REG} \text{ (-004 code, } 0\% / ^\circ\text{C)}$



V_{REG} is the IC's internal constant voltage source, whose voltage values (at $T_A = 25^\circ\text{C}$) are listed in Table 10-3 below.

Table 10-3. V_{REG}

Product Code	Temperature Gradient (%/°C)	V_{REG} (V)
-001	-0.05	2.08
-002	-0.1	1.84
-003	-0.15	1.62
-004	0	2.39

Given α as the electronic volume command value, when data is set to the 6-bit electronic volume register, one of 64 statuses is set. Values for α corresponding to various electronic volume register settings are listed in Table 10-4 below.

Table 10-4. α Values Determined by Electronic Volume Register Settings

D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	1	61
0	0	0	0	1	1	60
:	:	:	:	:	:	:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra is an on-chip resistance factor used for the V_{LC1} voltage regulator. This factor can be controlled among eight levels using the V_{LC1} voltage regulator resistance factor set command. Table 10-5 lists reference values for (1+Rb/Ra) which are set when 3-bit data is set to the V_{LC1} voltage regulator resistance factor register.

Table 10-5. Reference Values for (1 + Rb/Ra)

Register			Reference Value
D ₃	D ₂	D ₁	
0	0	0	3.5
0	0	1	4.0
0	1	0	4.5
0	1	1	5.0
1	0	0	5.5
1	0	1	6.0
1	1	0	6.5
1	1	1	7.0

10.3.2 When using external resistor (not using on-chip resistor for V_{LC1} voltage regulator)

Instead of using the on-chip resistor for the V_{LC1} voltage regulator (IRS pin = L), resistors (Ra' and Rb') can be added between V_{SS} and V_R and between V_R and V_{LC1} to set the LCD power supply voltage V_{LC1}. In such cases, the electronic volume function can be used to control the LCD power supply voltage V_{LC1} using commands to regulate the darkness of the LCD contents. The V_{LC1} voltage can be determined using equation 10-2 as within the range of V_{LC1} < V_{LCD}.

Equation 10-2.

$$V_{LC1} = (1 + \frac{Rb'}{Ra'})V_{EV}$$

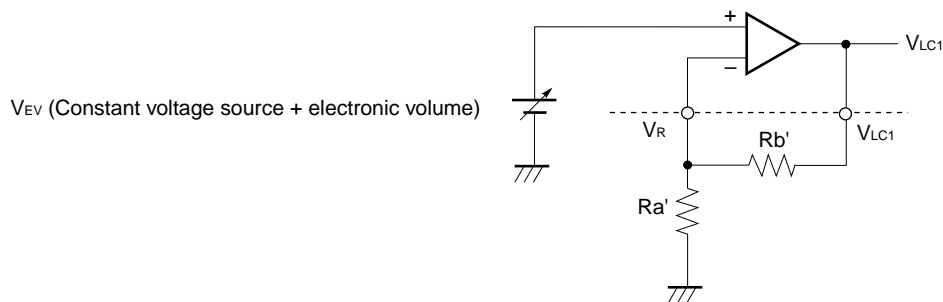
The equation for determining V_{EV} varies according to the product code (temperature gradient).

$$V_{EV} = \frac{162}{203} (1 - \frac{\alpha}{162}) V_{REG} \text{ (-001 code, } -0.05\% / ^\circ\text{C)}$$

$$V_{EV} = \frac{162}{178} (1 - \frac{\alpha}{162}) V_{REG} \text{ (-002 code, } -0.1\% / ^\circ\text{C)}$$

★
$$V_{EV} = (1 - \frac{\alpha}{162}) V_{REG} \text{ (-003 code, } -0.15\% / ^\circ\text{C)}$$

★
$$V_{EV} = \frac{162}{236} (1 - \frac{\alpha}{162}) V_{REG} \text{ (-004 code, } 0\% / ^\circ\text{C)}$$



10.4 Op Amp Control for Level Power Supply

The μ PD16682's on-chip power supply circuit is designed for low power consumption (HPM = H). Consequently, display quality may be diminished when a large LCD device or panel is used. In such cases, the display quality can be improved by setting HPM = L (high-power mode). We recommend that you check the actual display quality before deciding whether or not to use high-power mode.

If setting high-power mode still does not sufficiently improve the display quality, the LCD driver's power supply must be provided from an external source.

10.5 Command Sequence for Stepping Down On-chip Power Supply

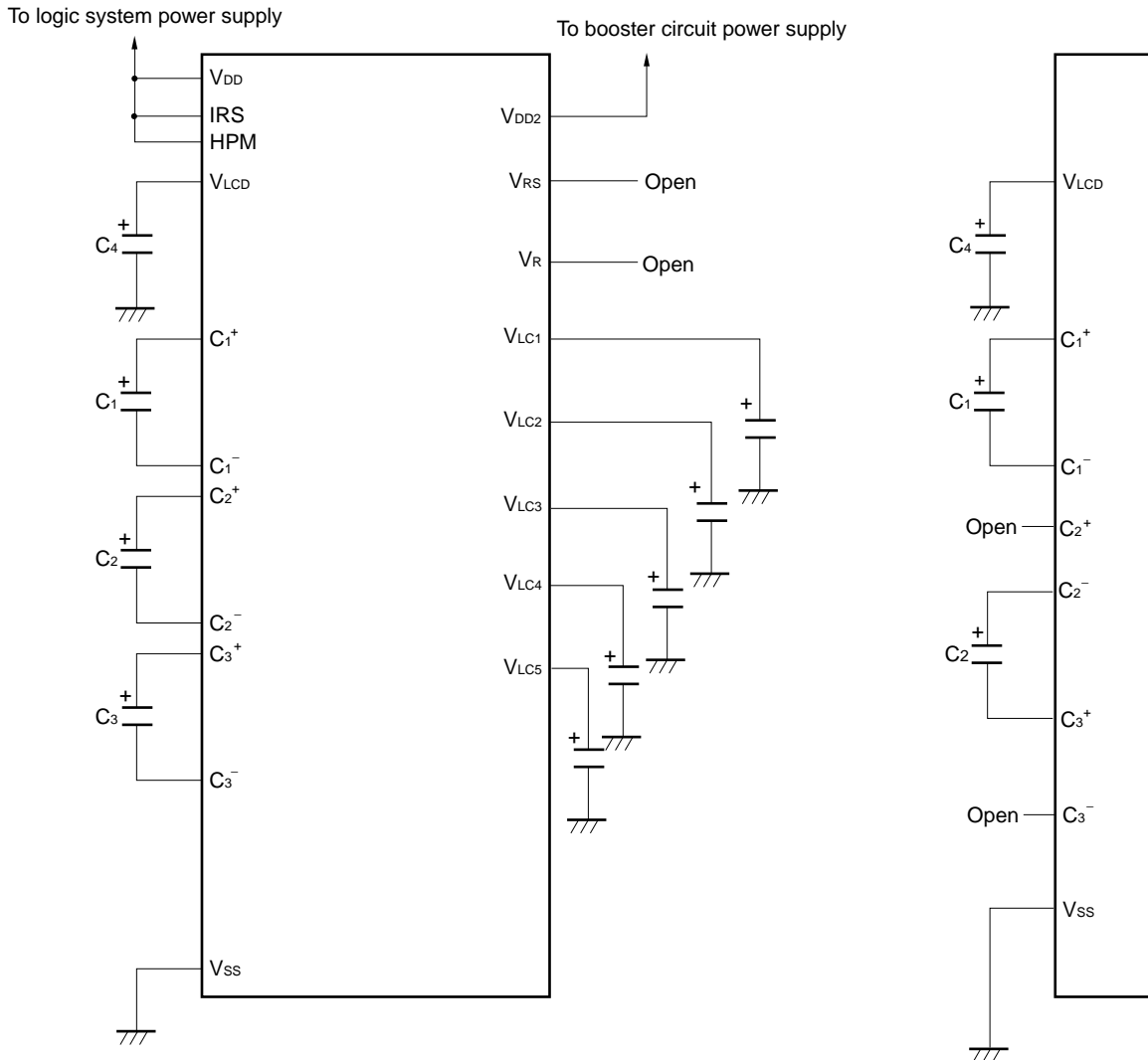
As shown in the following command sequence, we recommend that you set low power mode and turn off the power before stepping down the on-chip power supply.

Step	Description (Command, Status)	Command Address								
		D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Display OFF	1	0	1	0	1	1	1	0	} Power save command (compound)
Step2	Display all ON	1	0	1	0	0	1	0	1	
End	On-chip power supply OFF									

10.6 Use Example of Power Supply Circuit

A) 4x boost (normal mode/using on-chip power supply)

B) 3x boost



Note Leave the C₂⁺ and C₃⁻ pins open.

Remark C₁ = C₂ = C₃ = C₄ = 1.0 μ F

11. RESET CIRCUIT

In the μ PD16682, when the /RES input is at low level, a reset is executed. The reset (default) settings are described below.

1. Display OFF
2. Normal display direction
3. ADC select: normal direction (ADC command $D_0 = L$)
4. Power control register: $(D_2, D_1, D_0) = (0, 0, 0)$
5. Data cleared from register in serial interface
6. LCD power supply bias: 1/9 bias
7. Read modify write OFF
8. Power save canceled
9. SEG/COM output: V_{SS}
10. Static indicator OFF
Static indicator register: $(D_2, D_1) = (0, 0)$
11. Display start line: set to line 1
12. Column address: set to address 0
13. Page address: set to page 0
14. Common output status: Normal
15. Canceled mode set for on-chip resistance factor for V_{LC1} voltage regulator
 V_{LC1} voltage regulator resistance factor register $(D_2, D_1, D_0) = (0, 0, 0)$
16. Canceled mode set for electronic volume register
Electronic volume register: $(D_5, D_4, D_3, D_2, D_1, D_0) = (1, 0, 0, 0, 0, 0)$
17. Test mode canceled
18. Display all OFF (display all ON/OFF command, $D_0 = L$)

Only items 1, 7, and 9 to 18 above are executed when a reset command is used.

12. COMMANDS

The μ PD16682 uses a combination of A0, /RD(E), and /WR(R,/W) to identify data bus signals. Command interpretation and execution is performed using internal timing that does not depend on any external clock.

The 80 series MPU interface activates commands using low pulse input to the /RD pin during read and activates commands using low pulse input to the /WR pin during write. The 68 series MPU interface sets read mode using high-level input to the R,/W pin and sets write mode using low-level input to the R,/W pin. The command is activated using high pulse input to the E pin.

Thus, the 68 series MPU interface differs from the 80 series MPU interface in that /RD(E) is at high level during status read and display data read operations, as is shown in the command descriptions and command table.

Command descriptions using an 80 series MPU interface are shown below.

If the serial interface has been selected, data is input sequentially starting from D7.

12.1 Display ON/OFF

This command specifies the display's ON/OFF status.

A0	E, /RD	R,/W, /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

Executing the display all ON command while the display is OFF sets power save (low power) mode. For details, see

12.20 Power Save (Compound Command).

When the display is OFF, output via all driver outputs (segment and common) is at V_{SS} level.

12.2 Display Start Line Set

This command specifies the address of the display start line in the display data RAM, as was shown in Figure 6-2. The display area extends from the specified line address in the direction of higher line addresses, and includes the number of lines that corresponds to the display duty setting. The display can be smoothly scrolled vertically by using this command to dynamically modify the specified line addresses.

For details, see **6.4 Line Address Circuit**.

A0	E, /RD	R,/W, /WR	D7	D6	D5	D4	D3	D2	D1	D0	Line Address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

12.3 Page Address Set

This command specifies the page address corresponding to the row address when accessing the display data RAM from the MPU side, as was shown in Figure 6-2. The specified bit in display data RAM can be accessed by selecting the corresponding page address and column address. If the page address is changed, the display mode does not change.

For details, see **6.2 Page Address Circuit**.

A0	E, /RD	R, /W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Page Address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
									↓		↓
							0	1	1	1	7
							1	0	0	0	8

12.4 Column Address Set

This command specifies the column address in display data RAM, as was shown in Figure 6-2. The column address is set in a (basically continuous) series of two specifications, one for the high-order four bits and another for the low-order four bits. The column address is automatically incremented (+1) each time the display data RAM is accessed, so the MPU is able to continuously read or write display data. Incrementation of the column address stops at 83H. At that point the page address can no longer be continuously modified. For details, see **6.3 Column Address Circuit**.

A0	E, /RD	R, /W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	0	0	1	A7	A6	A5	A4
						0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
				↓				↓
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

12.5 Status Read

A0	E, /RD	R,/W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	ADC	ON/OFF	RESET	0	0	0	0

ADC	This indicates the relation between the column address and the segment driver. 0: Inverted (column address 131-n ↔ SEGn) 1: Normal (column address n ↔ SEGn)
ON/OFF	ON/OFF: Indicates the display's ON/OFF status. 0: Display ON 1: Display OFF (This is the opposite of the display ON/OFF command's polarity.)
RESET	This indicates whether or not the system is undergoing a reset via the /RES signal or the reset command. 0: Operating mode 1: Reset in progress

12.6 Display Data Write

This command writes 8 bits of data to the specified address in display data RAM. After this data has been written, the column address is automatically incremented (+1), which enables the MPU to continuously write display data.

A0	E, /RD	R,/W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	Write Data							

12.7 Display Data Read

This command reads 8 bits of data from the specified address in display data RAM. After this data has been read, the column address is automatically incremented (+1), which enables the MPU to continuously read several words of data.

A single dummy read operation is required immediately after the column address has been set. For details, see

5.1.5 Display data RAM and internal register access.

Note that the display data cannot be read when using a serial interface.

A0	E, /RD	R,/W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	Read Data							

12.8 ADC Select (Segment Driver Direction Select)

This command inverts the relation between the display data RAM's column address and segment driver output, as was shown in Figure 6-2. Consequently, the segment driver output pin number can be inverted by this command. For details, see **6.3 Column Address Circuit**. Incrementation (+1) of the column address when display data is either written or read is performed according to the column address shown in Figure 6-2.

This command should be input during initialization.

A0	E, /RD	R, /W, /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	1	0	0	0	0	Normal (forward direction)
										1	Inverted (reverse direction)

12.9 Display Normal/Inverted

This command can be used to invert the display ON/OFF control without replacing any of the display data RAM contents. The display data RAM contents are retained when this command is executed.

A0	E, /RD	R, /W, /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM data: H LCD ON potential (normal)
										1	RAM data: L LCD ON potential (inverted)

12.10 Display All ON/OFF

This command can be used to set the display all ON status forcibly regardless of the display data RAM contents. The display data RAM contents are retained when this command is executed.

This command takes priority over the display normal/inverted command.

A0	E, /RD	R, /W, /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all ON

12.11 LCD Bias Set

This command selects the bias setting of the voltage required to drive the LCD. This command is valid when the power supply circuit's V/F circuit is operating.

A0	E, /RD	R, /W, /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	1	0	1/9 bias
										1	1/7 bias

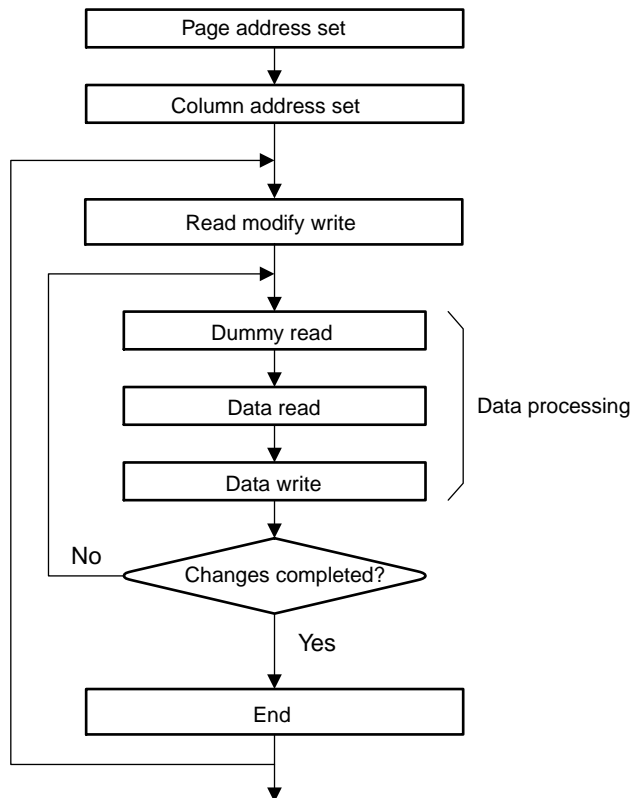
12.12 Read Modify Write

This command is used in a pair with the end command. When this command has been input, the column address is not changed by the display data read command and can be incremented (+1) only by the display data write command. This status is retained until an end command is input. Once an end command has been input, the column address returns to the address that was used when the read modify write command was input. This function can be used to lighten the burden on the MPU when repeatedly modifying data in special display areas such as the blinking cursor.

A0	E, /RD	R,/W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	1	1	0	0	0	0	0

Caution The commands other than the display data read/write commands can be used even during read modify write mode. However, the column address set command cannot be used.

Figure 12-1. Sequence for Cursor Display

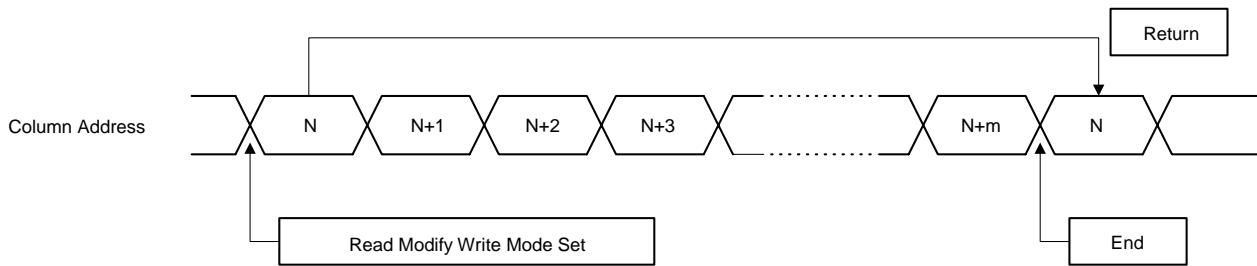


12.13 End

This command is used to cancel read modify write mode and return to the address that was used during column address mode reset.

A0	E, /RD	R,/W, /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Figure 12-2. End



12.14 Reset

This command initializes the contents of the various command registers. The display data RAM is not affected. For details, see 11. **RESET CIRCUIT.**

The reset operation is performed after the reset command has been input.

A0	E, /RD	R,/W, /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The reset that occurs when the power supply is applied is performed by issuing a reset signal to the /RES pin. It cannot be used as a substitute for the reset command.

12.15 Common Output Status Select

This command can be used to select the scan direction for the COM output pins. For details, see 9. **COMMON OUTPUT STATUS SELECT CIRCUIT.**

A0	E, /RD	R,/W, /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	0	0	0	X	X	X	Normal (forward)
							1				Inverted (reverse)

Remark X: Don't care

Status	Selected status	
Normal (forward)	COM ₀	→ COM ₆₃
Inverted (reverse)	COM ₆₃	→ COM ₀

12.16 Power Control Set

This command is used to set the function of the power supply circuit. For further description, see **10. POWER SUPPLY CIRCUIT**.

A0	E, /RD	R, /W, /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Status
0	1	0	0	0	1	0	1	0	X	X	Booster circuit: OFF
								1	X	X	Booster circuit: ON
								X	0	X	V regulator circuit: OFF
								X	1	X	V regulator circuit: ON
								X	X	0	V/F circuit: OFF
								X	X	1	V/F circuit: ON

Remark X: Don't care

12.17 Set On-chip Resistance Factor for V_{LC1} Voltage Regulator

This command is used to set the on-chip resistance factor for the V_{LC1} voltage regulator. For details, see **10.3 Voltage Regulator Circuit**.

A0	E, /RD	R, /W, /WR	D7	D6	D5	D4	D3	D2	D1	D0	(1+Rb/Ra)
0	1	0	0	0	1	0	0	0	0	0	3.5
								0	0	1	4.0
								0	1	0	4.5
								0	1	1	5.0
								1	0	0	5.5
								1	0	1	6.0
								1	1	0	6.5
								1	1	1	7.0

12.18 Electronic Volume (Two-Byte Command)

This command can be used to control the LCD drive voltage V_{LC1} (which is output from the on-chip LCD power supply's voltage regulator circuit) to regulate the darkness of the LCD contents.

This command is a two-byte command that is used in a pair with the electronic volume mode set command and the electronic volume register set command, so be sure to use both commands consecutively.

12.18.1 Electronic volume mode set command (first byte)

Once this command is input, the electronic volume register set command becomes valid. And once the electronic volume mode has been set, any command other than the electronic volume register set command cannot be used. This restriction is cleared once data has been set to the register by the electronic volume register set command.

A0	E, /RD	R, /W, /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

12.18.2 Electronic volume register set command (second byte)

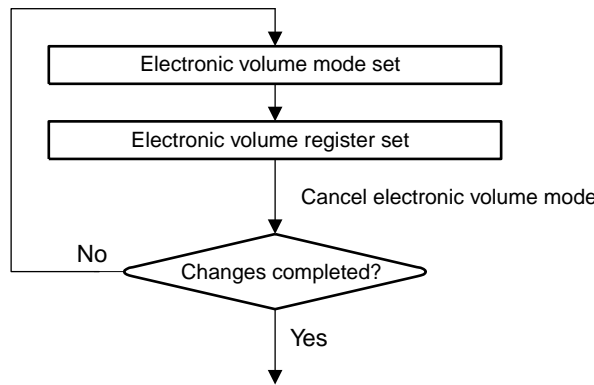
When six bits of data are set to the electronic volume register by this command, the LCD drive voltage V_{LC1} is set to one of 64 possible voltage values.

Once this command has been input and the electronic volume register has been set, electronic volume mode is canceled.

A0	E, /RD	R, /W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	V_{LC1}	
0	1	0	X	X	0	0	0	0	0	0	Smaller value	
			X	X	0	0	0	0	0	1		
			X	X	0	0	0	0	1	0		
												↓
			X	X	1	1	1	1	1	1	0	
			X	X	1	1	1	1	1	1	1	Larger value

Remark X: Don't Care

Figure 12-3. Sequence of Electronic Volume Register Set Operations



12.19 Static Indicator (Two-Byte Command)

This command is used to control the indicator display for the static drive system. Only this command can control the static indicator display, and it operates independently of other display control commands.

One of the electrodes for the static indicator's LCD driver is connected to the FR pin and the other is connected to the FRS pin. We recommend that these status indicator electrodes be implemented in a pattern that is separate from the electrodes used for the dynamic drive. The LCD and the electrodes themselves may deteriorate if the patterns are laid out too close to each other.

The static indicator ON command is a two-byte command that is used in a pair with the static indicator register set command, so be sure to use both commands consecutively. (The static indicator OFF command is a one-byte command.)

12.19.1 Static indicator ON/OFF

When the static indicator ON command is input, the static indicator register set command becomes valid. Once the static indicator ON command has been input, any command other than the static indicator register set command cannot be used. This restriction is cleared once data has been set to the register by the static indicator register set command.

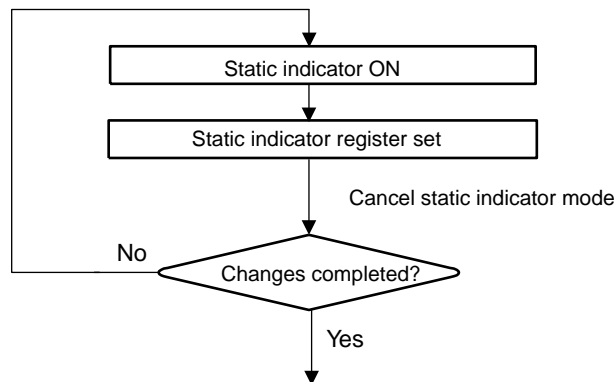
A0	E, /RD	R, /W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

12.19.2 Static indicator register set

This command sets data to the two-bit static indicator register and then sets the static indicator to blink mode.

A0	E, /RD	R, /W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Static Indicator
0	1	0	X	X	X	X	X	X	0	0	OFF
									0	1	ON (blinks at one-second interval)
									1	0	ON (blinks at half-second interval)
									1	1	ON (always ON)

Figure 12-4. Sequence of Static Indicator Register Set Operations



12.20 Power Save (Compound Command)

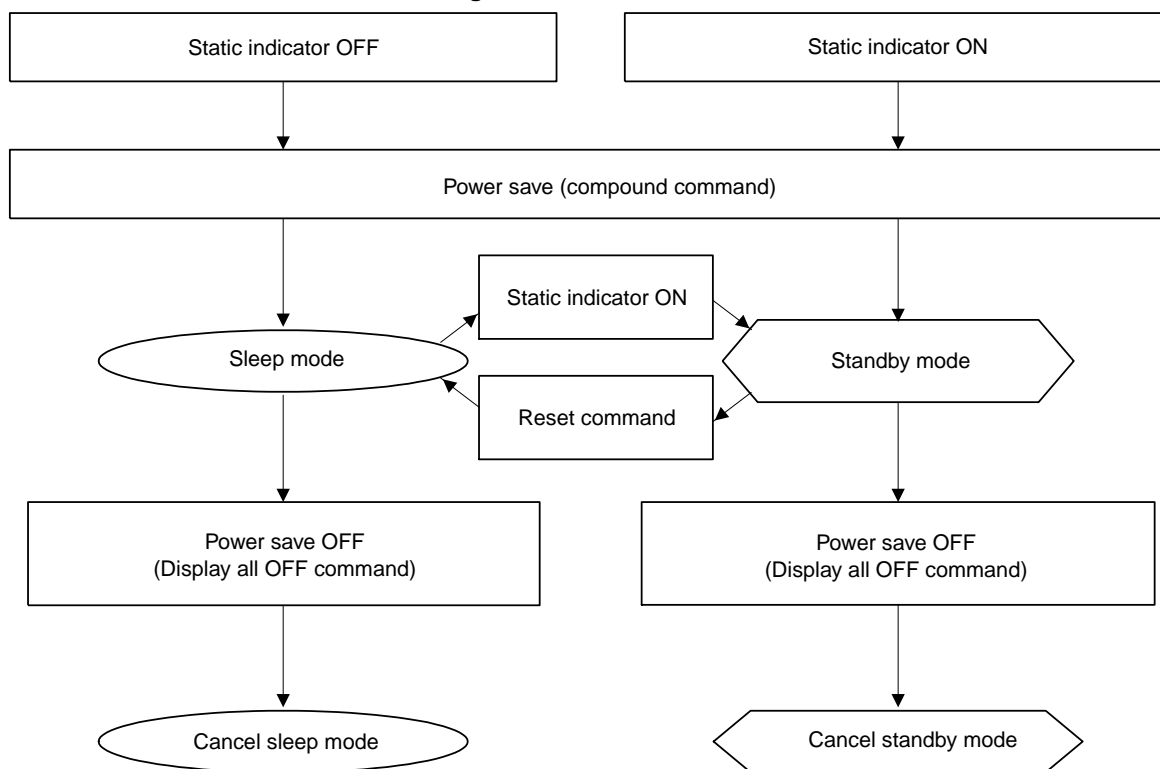
The current consumption can be greatly reduced by entering the power save status by inputting the display all ON command while the display is in OFF mode.

The power save (low power) mode includes two modes; sleep mode and standby mode. Turning the static indicator OFF sets sleep mode and turning it ON sets standby mode.

During either sleep mode or standby mode, the display data is retained as it was before the power save function was activated. Also, access to the display data RAM from the MPU is possible during either mode.

Use the display all OFF command to cancel power save mode.

Figure 12-5. Power Save



12.20.1 Sleep mode

During this mode, all LCD operations are stopped and there is no access from the MPU, so current consumption can be reduced almost as low as the static current level. The internal status during sleep mode is as follows.

- (1) The oscillation circuit and LCD power supply circuit are stopped.
- (2) All LCD drive circuits are stopped and both segment and common driver outputs output at the V_{ss} level.

12.20.2 Standby mode

During this mode, all duty LCD display system operations are stopped and only the static drive system for the indicators operate, which reduces the current consumption to the minimum amount needed for static drive. The internal status during standby mode is as follows.

- (1) The LCD's power supply circuit is stopped. The oscillation circuit operates.
- (2) The duty drive system's LCD drive circuit is stopped and both segment and common driver outputs output at the V_{ss} level. The static drive system operates.

When a reset command is executed while in standby mode, it sets sleep mode.

- Remarks 1.** If you are using an external power supply, we recommend that you stop the external power supply circuit's functions when activating the power save function. For example, if you are using an external divided resistor circuit to provide LCD drive voltage at different levels, we recommend that you add a circuit to cut the current flowing on the divided resistor circuit while the power save function is being activated.
- 2.** The μ PD16682 includes the /DOF pin which is used to control blinking LCD displays is set to low level when activating the power save function. The output from /DOF can be used to stop the external power supply circuit's function.
- 3.** When the display has been set to OFF mode, executing the display all ON command sets power save mode no matter which command is entered afterward.

12.21 NOP

This command is used to set NOP (Non-Operation) mode.

A0	E, /RD	R,/W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	1	1	0	0	0	1	1

12.22 Test

This command is used for IC testing. Do not use this command. If you use it by mistake, either set the /RES input low or use the reset command or NOP command to cancel the test command setting.

A0	E, /RD	R,/W, /WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	1	1	1	X	X	X	X

Remark X: Don't care

Table 12-1. List of μ PD16682 Commands (1/2)

Command	Command code											Function	
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0		
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	1	Sets LCD's ON/OFF status 0: OFF, 1: ON
Display start line set	0	1	0	0	1	Display start address					Sets display RAM's display start line address		
Page address set	0	1	0	1	0	1	1	Page address				Sets display RAM's page address	
Column address set (high-order bits)	0	1	0	0	0	0	1	High-order column address				Sets high-order four bits of display RAM's column address	
Column address set (low-order bits)	0	1	0	0	0	0	0	Low-order column address					
Status read	0	0	1	0	Status			0	0	0	0	Read status information	
Display data write	1	1	0	Write data								Writes to display RAM	
Display data read	1	0	1	Read data								Reads from display RAM	
ADC select	0	1	0	1	0	1	0	0	0	0	0	1	Sets correspondence of SEG output to display RAM address 0: Normal, 1: Inverted
Display normal/inverted	0	1	0	1	0	1	0	0	1	1	0	1	Sets normal/inverted direction of display
Display all ON/OFF	0	1	0	1	0	1	0	0	1	0	0	1	Sets display all ON 0: Normal display, 1: All ON
LCD bias set	0	1	0	1	0	1	0	0	0	1	0	1	Sets the bias setting of the LCD drive voltage 0: 1/9 bias, 1: 1/7 bias
Read modify write	0	1	0	1	1	1	0	0	0	0	0	0	Specifies incrementation of the column address During write: +1, During read: 0
End	0	1	0	1	1	1	0	1	1	1	0	0	Cancels read modify write
Reset	0	1	0	1	1	1	0	0	0	0	1	0	Sets an internal reset
Selects scan direction for COM outputs	0	1	0	1	1	0	0	0	1	X	X	X	Sets scan direction for COM outputs 0: Normal (forward), 1: Inverted (reverse)

Table 12–1. List of μPD16682 Commands (2/2)

Command	Command code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
Power control set	0	1	0	0	0	1	0	1	Operation mode			Selects operation mode of internal power supply
Sets V _{LC1} output voltage to electronic volume register	0	1	0	0	0	1	0	0	Resistance factor setting			Selects on-chip resistance factor for (Ra/Rb)
Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Sets V _{LC1} output voltage to electronic volume register
Electronic volume register set	0	1	0	X	X	Electronic volume value						
Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	0: OFF, 1: ON
Static indicator register set	0	1	0	X	X	X	X	X	X	Mode		
Power save												Compound command for setting display OFF and all display ON
NOP	0	1	0	1	1	1	0	0	0	1	1	Command for Non-Operation mode
Test	0	1	0	1	1	1	1	X	X	X	X	Command used for IC testing Caution Do not use this command.

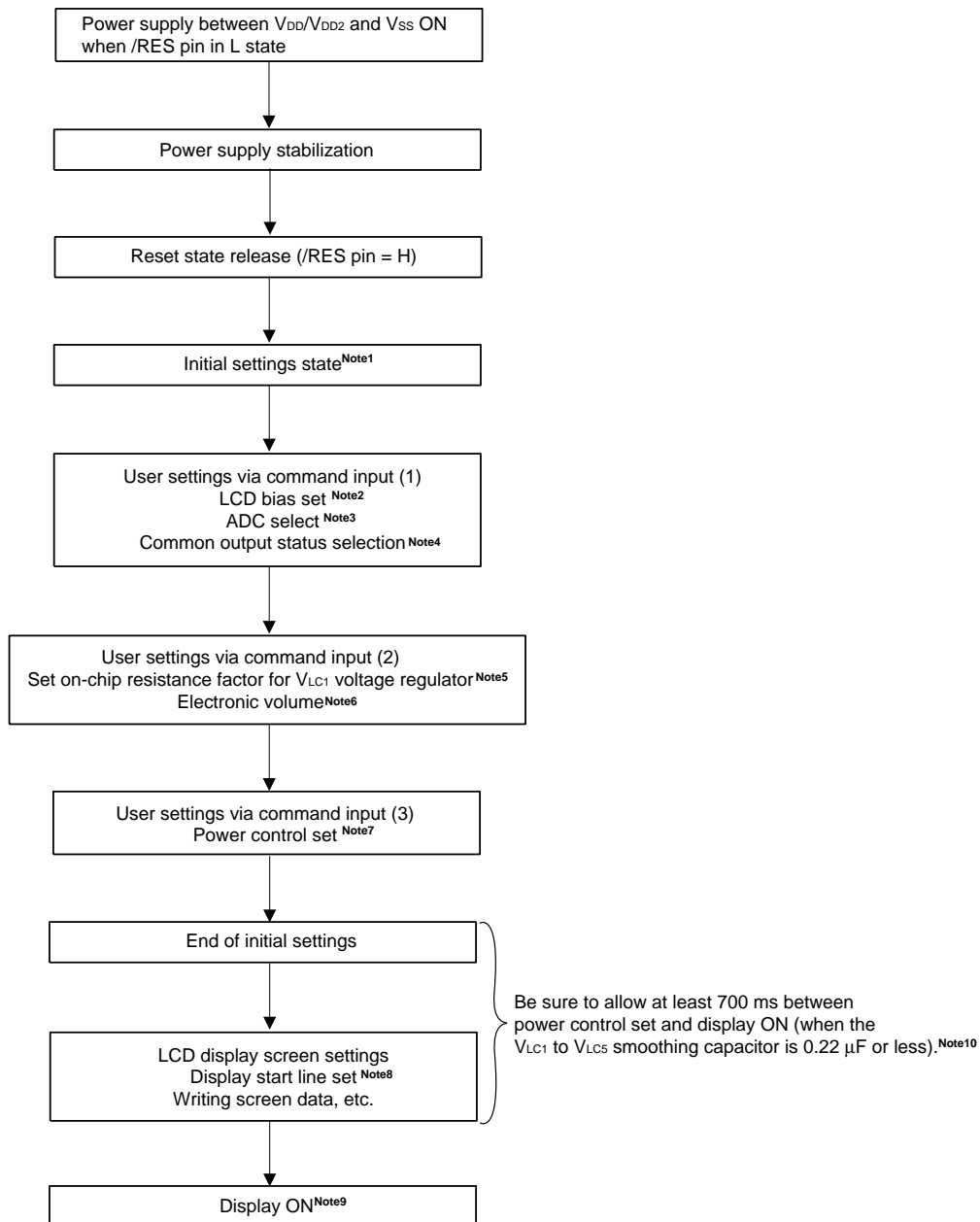
Remark X: Don't care

13. ACCESS PROCEDURE

13.1 Initialization setting example (from power application to display ON)

Although a V_{SS} level is output from the SEG and COM LCD drive output pins when power is applied to the IC, if there is electric charge remaining in the smoothing capacitor connected between the driver reference power supply pins (V_{LC1} to V_{LC5}) and V_{SS} , or if the DC/DC converter's booster voltage does not reach the prescribed booster potential or the levels of the reference power supplies (V_{LCn}) do not reach the prescribed voltages when power is applied, abnormalities such as a temporary screen blackout may occur when the display turns on.

The following power application flow is recommend to avoid the occurrence of abnormal operation when the power is turned on.



Notes 1. See 11. RESET CIRCUIT.

2. See 12.11 LCD Bias Set.

3. See 12.8 ADC Select (Segment Driver Direction Select).

4. See 12.15 Common Output Status Select.

5. See 12.17 Set On-chip Resistance Factor for V_{LC1} Voltage Regulator.

6. See 12.18 Electronic Volume (Two-Byte Command).

7. See 12.16 Power Control Set.

8. See 12.2 Display Start Line Set.

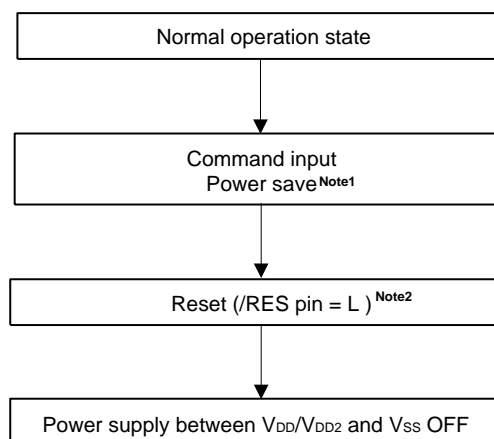
9. See 12.1 Display ON/OFF.

10. This period changes depending on the panel characteristics and the capacitance of the booster/smoothing capacitor. It is recommended to determine this value after sufficient evaluation using the actual device.

13.2 Example of power OFF

When turning the power of the IC off in the normal operation state (liquid crystal display ON, on-chip power supply circuits operating), because there is electric charge remaining in the power supply level smoothing capacitor connected between the driver reference power supply pins (V_{LC1} to V_{LC5}) and V_{SS} , power continues to be supplied to the LCD drive circuit and voltage may be applied to the LCD panel from the SEG and COM pins. At this time, the LCD panel may momentarily display data.

Moreover, because the visual quality of the LCD panel may be affected, be sure to turn off the power to the IC in the following sequence.



Notes 1. See 12.20 Power Save (Compound Command).

2. Application of a reset is optional.

14. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{DD}	-0.3 to +6.0	V
Supply voltage 2 (4x boost)	V _{DD2}	-0.3 to +3.75	V
Supply voltage 2 (3x boost)	V _{DD2}	-0.3 to +5.0	V
Driver supply voltage	V _{LCD}	-0.3 to +15.0, V _{DD} ≤ V _{LCD}	V
Driver reference supply input voltage	V _{LC1-VLC5}	-0.3 to V _{LCD} +0.3	V
Logic system input voltage	V _{IN1}	-0.3 to V _{DD} +0.3	V
Logic system output voltage	V _{OUT1}	-0.3 to V _{DD} +0.3	V
Logic system input/output voltage	V _{I/O1}	-0.3 to V _{DD} +0.3	V
Driver system input voltage	V _{IN2}	-0.3 to V _{LCD} +0.3	V
Driver system output voltage	V _{OUT2}	-0.3 to V _{LCD} +0.3	V
Operating ambient temperature	T _A	-40 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
★ Supply voltage	V _{DD}	2.4		4.5	V
Supply voltage 2 (4x boost)	V _{DD2}	2.4		3.0	V
Supply voltage 2 (3x boost)	V _{DD2}	2.4		4.0	V
Driver supply voltage	V _{LCD}	6	10	12	V
Logic system input voltage	V _{IN}	0		V _{DD}	V
Driver system input voltage	V _{LC1-VLC5}	0		V _{LCD}	V

Remarks 1. When using an external power supply, be sure to maintain these relations:

$$V_{SS} < V_{LC5} < V_{LC4} < V_{LC3} < V_{LC2} < V_{LC1} \leq V_{LCD}$$

2. Maintain V_{DD} ≤ V_{LCD} when turning the power on or off.

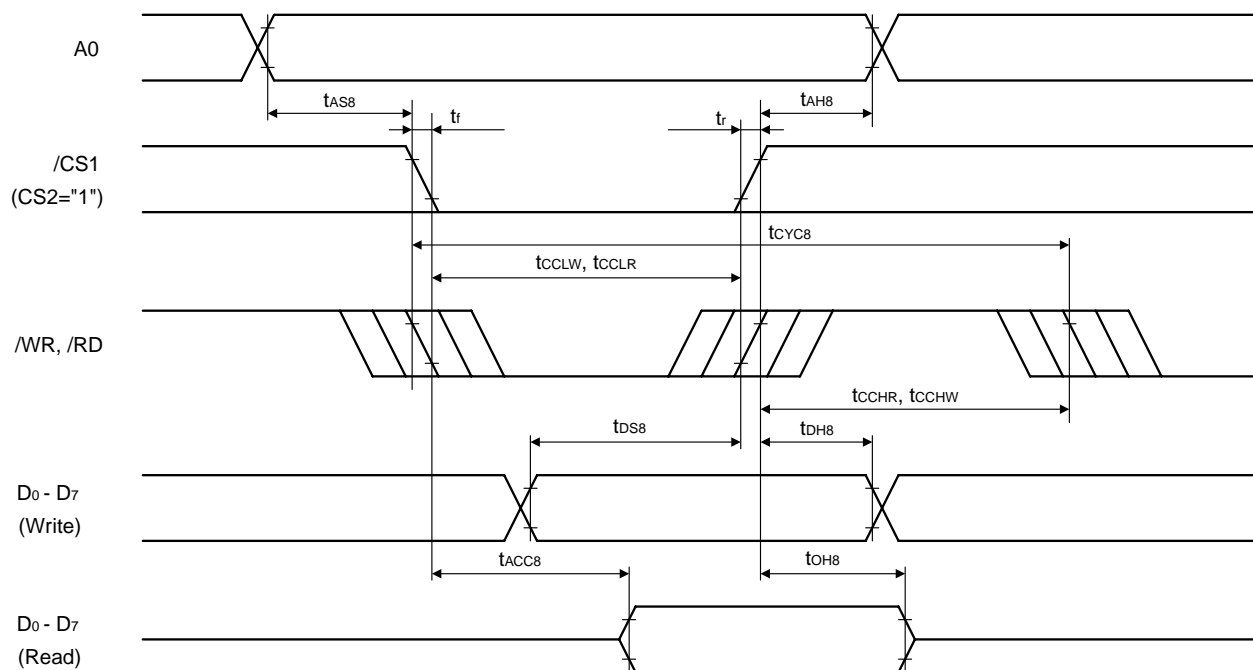
Electrical Characteristics (unless otherwise specified, T_A = -40 to +85 °C, V_{DD2} = 2.7 to 3.3 V, during 4x boost mode: V_{DD2} = 2.7 to 3.0 V, or during 3x boost mode: V_{DD2} = 2.7 to 4.0 V)

Parameter	Symbol	Condition	MIN.	TYP. ^{Note}	MAX.	Unit
High-level input voltage	V _{IH}		0.8 V _{DD}			V
Low-level input voltage	V _{IL}				0.2 V _{DD}	V
High-level input current	I _{IH1}	Except for D ₇ (SI), D ₆ (SCL), and D ₅ to D ₀			1	μA
Low-level input current	I _{IL1}	Except for D ₇ (SI), D ₆ (SCL), and D ₅ to D ₀			-1	μA
High-level output voltage	V _{OH}	I _{OUT} = -1.5 mA, except OSC _{OUT}	V _{DD} - 0.5			V
Low-level output voltage	V _{OL}	I _{OUT} = 4 mA, except OSC _{OUT}			0.5	V
High-level leakage current	I _{LOH}	D ₇ (SI), D ₆ (SCL), and D ₅ to D ₀ V _{IN/OUT} = V _{DD}			10	μA
Low-level leakage current	I _{LOL}	D ₇ (SI), D ₆ (SCL), and D ₅ to D ₀ V _{IN/OUT} = V _{SS}			-10	μA
Common output ON resistance	R _{COM}	V _{LCDn} → COM _n , V _{LCD} ≥ 3V _{DD2} , I _{LOL} = 50 μA			2	kΩ
Segment output ON resistance	R _{SEG}	V _{LCDn} → SEG _n , V _{LCD} ≥ 3V _{DD2} , I _{LOL} = 50 μA			4	kΩ
Driver voltage (boost voltage)	V _{LCD}	During 3x boost	2.7 V _{DD}		3.0 V _{DD}	V
		During 4x boost	3.6 V _{DD}		4.0 V _{DD}	V
Current consumption (normal mode)	I _{DD11}	f _{OSC} = 22 kHz, all display OFF data output, V _{DD} = V _{DD2} = 3.0 V during 3x boost mode, T _A = 25 °C		55	110	μA
		f _{OSC} = 22 kHz, all display OFF data output, V _{DD} = V _{DD2} = 3.0 V during 4x boost mode, T _A = 25 °C		78	135	μA
		f _{OSC} = 22 kHz, checker pattern data output, V _{DD} = V _{DD2} = 3.0 V during 3x boost mode, T _A = 25 °C		90	140	μA
		f _{OSC} = 22 kHz, checker pattern data output, V _{DD} = V _{DD2} = 3.0 V during 4x boost mode, T _A = 25 °C		160	210	μA
Current consumption (high-power mode)	I _{DD12}	f _{OSC} = 22 kHz, all display OFF data output, V _{DD} = V _{DD2} = 3.0 V during 3x boost mode, T _A = 25 °C		104	190	μA
		f _{OSC} = 22 kHz, all display OFF data output, V _{DD} = V _{DD2} = 3.0 V during 4x boost mode, T _A = 25 °C		153	230	μA
		f _{OSC} = 22 kHz, checker pattern data output, V _{DD} = V _{DD2} = 3.0 V during 3x boost mode, T _A = 25 °C		130	215	μA
		f _{OSC} = 22 kHz, checker pattern data output, V _{DD} = V _{DD2} = 3.0 V during 4x boost mode, T _A = 25 °C		210	290	μA
Current consumption (standby mode)	I _{DD21}	f _{OSC} = 22 kHz, V _{DD} = V _{DD2} = 3.0 V, T _A = 25 °C		7	15	μA
Current consumption (sleep mode)	I _{DD22}	all display OFF data output, V _{DD} = V _{DD2} = 3.0 V		0.2	5	μA
Oscillation frequency	f _{OSC}	T _A = 25 °C, V _{DD} = V _{DD2} = 3.0 V ± 10 %	17	22	25	kHz

Note The TYP. value is a reference value when T_A = 25 °C

Required timing conditions (unless otherwise specified, T_A = -40 to +85 °C)

80 Series MPU



(V_{DD} = 2.7 to 4.5 V)

Parameter	Symbol	Conditions	MIN.	TYP. ^{Note}	MAX.	Unit
Address hold time	t _{AH8}	A0	0			ns
Address setup time	t _{AS8}	A0	0			ns
System cycle time	t _{CYC8}		300			ns
Control L pulse width (/WR)	t _{CCLW}	/WR	60			ns
Control L pulse width (/RD)	t _{CCLR}	/RD	120			ns
Control H pulse width (/WR)	t _{CCHW}	/WR	60			ns
Control H pulse width (/RD)	t _{CCHR}	/RD	60			ns
Data setup time	t _{DS8}	D ₀ to D ₇	40			ns
Data hold time	t _{DH8}	D ₀ to D ₇	15			ns
/RD access time	t _{ACC8}	D ₀ to D ₇ , C _L = 100 pF			140	ns
Output disable time	t _{OH8}	D ₀ to D ₇ , C _L = 100 pF	10		100	ns

Note The TYP. value is a reference value when T_A = 25 °C

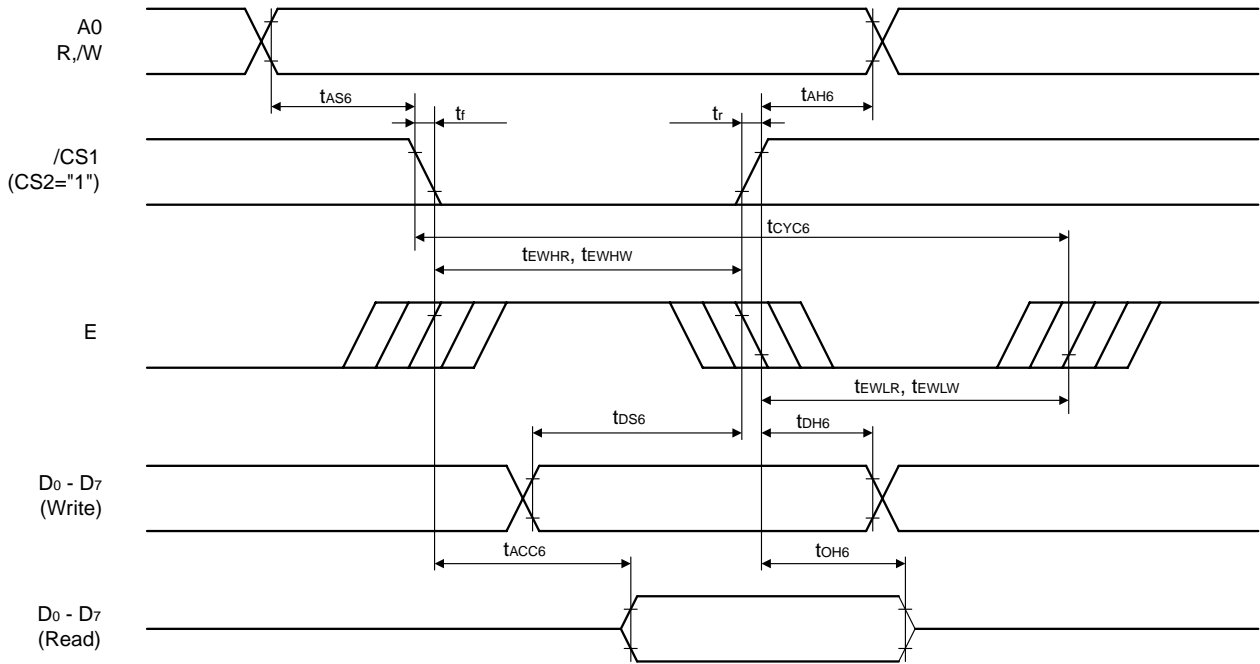
(V_{DD} = 2.4 to 2.7 V)

Parameter	Symbol	Conditions	MIN.	TYP. ^{Note}	MAX.	Unit
Address hold time	t _{AH8}	A0	0			ns
Address setup time	t _{AS8}	A0	0			ns
System cycle time	t _{CYC8}		1000			ns
Control L pulse width (/WR)	t _{CCLW}	/WR	120			ns
Control L pulse width (/RD)	t _{CCLR}	/RD	240			ns
Control H pulse width (/WR)	t _{CCHW}	/WR	120			ns
Control H pulse width (/RD)	t _{CCHR}	/RD	120			ns
Data setup time	t _{DS8}	D ₀ to D ₇	80			ns
Data hold time	t _{DH8}	D ₀ to D ₇	30			ns
/RD access time	t _{ACC8}	D ₀ to D ₇ , C _L = 100 pF			280	ns
Output disable time	t _{OH8}	D ₀ to D ₇ , C _L = 100 pF	10		200	ns

Note The TYP. value is a reference value when T_A = 25 °C

- Remarks**
1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either (t_r + t_f) < (t_{CYC8} - t_{CCLW} - t_{CCHW}) or (t_r + t_f) < (t_{CYC8} - t_{CCLR} - t_{CCHR}).
 2. All timing is rated based on 20 % or 80 % of V_{DD}.
 3. t_{CCLW} and t_{CCLR} are rated as the overlap time when /CS1 is at low level (CS2 = H) and /WR and /RD are also at low level.

68 Series MPU



($V_{DD} = 2.7$ to 4.5 V)

Parameter	Symbol	Conditions	MIN.	TYP. ^{Note}	MAX.	Unit
Address hold time	t_{AH6}	A0	0			ns
Address setup time	t_{AS6}	A0	0			ns
System cycle time	t_{CYC6}		300			ns
Data setup time	t_{DS6}	D ₀ to D ₇	40			ns
Data hold time	t_{DH6}	D ₀ to D ₇	15			ns
Access time	t_{ACC6}	D ₀ to D ₇ , $C_L = 100$ pF			140	ns
Output disable time	t_{OH6}	D ₀ to D ₇ , $C_L = 100$ pF	10			ns
Enable H pulse width	Read	t_{EWHR} E	120			ns
	Write	t_{EWHW} E	60			ns
Enable L pulse width	Read	t_{EHLR} E	60			ns
	Write	t_{EHLW} E	60			ns

Note The TYP. value is a reference value when $T_A = 25$ °C

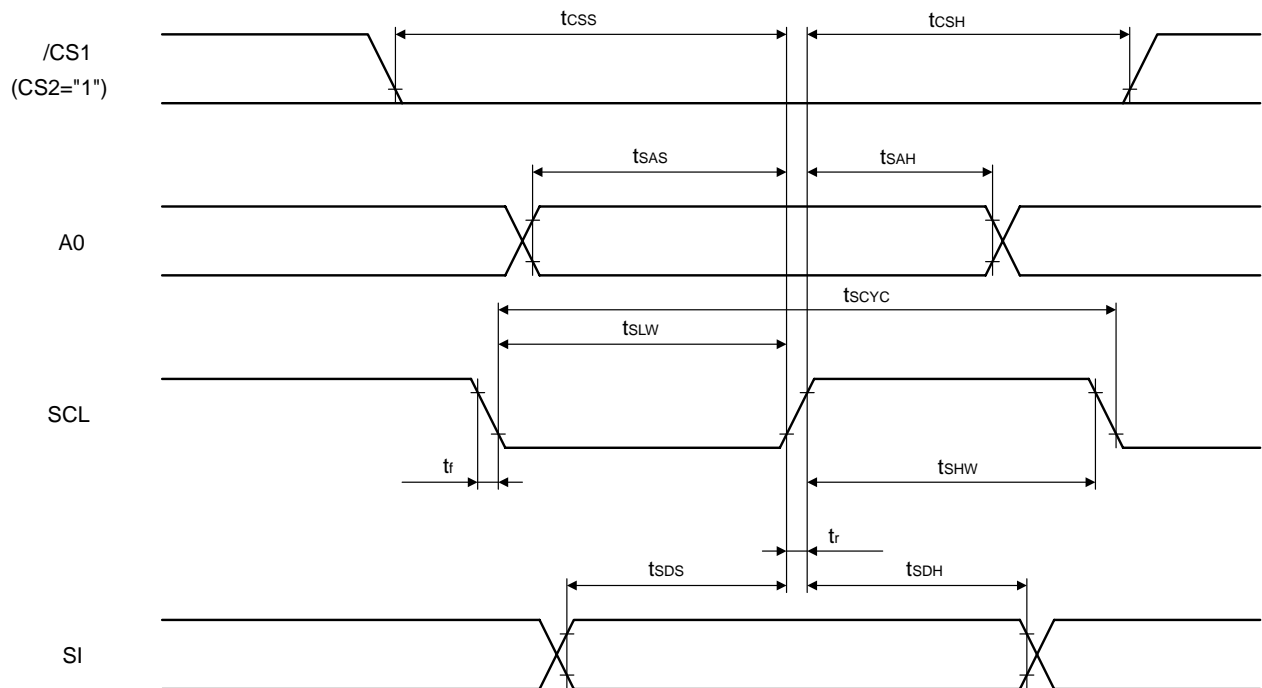
(V_{DD} = 2.4 to 2.7 V)

Parameter	Symbol	Conditions	MIN.	TYP. ^{Note}	MAX.	Unit
Address hold time	t _{AH6}	A0, R,/W	0			ns
Address setup time	t _{AS6}	A0, R,/W	0			ns
System cycle time	t _{CYC6}		1000			ns
Data setup time	t _{DS6}	D ₀ to D ₇	80			ns
Data hold time	t _{DH6}	D ₀ to D ₇	30			ns
Access time	t _{ACC6}	D ₀ to D ₇ , C _L = 100 pF			280	ns
Output disable time	t _{OH6}	D ₀ to D ₇ , C _L = 100 pF	10			ns
Enable H pulse width	Read	t _{EWHR}	E	240		ns
	Write	t _{EWHW}	E	120		ns
Enable L pulse width	Read	t _{EWLR}	E	120		ns
	Write	t _{EWLW}	E	120		ns

Note The TYP. value is a reference value when T_A = 25 °C

- Remarks**
1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either (t_r + t_f) ≤ (t_{CYC6} - t_{EWLW} - t_{EWHW}) or (t_r + t_f) ≤ (t_{CYC6} - t_{EWLR} - t_{EWHR}).
 2. All timing is rated based on 20 % or 80 % of V_{DD}.
 3. t_{EWHW} and t_{EWLW} are rated as the overlap time when /CS1 is at low level (CS2 = H) and E is at high level.
 4. D₀ to D₇ change to output regardless of the state of the E signal when R,/W becomes H in the state of /CS1 = L, CS2 = H (See 5.1.2. (2) 68 Series Parallel Interface.).

Serial Interface



($V_{DD} = 2.7$ to 4.5 V)

Parameter	Symbol	Conditions	MIN.	TYP. ^{Note}	MAX.	Unit
Shift clock cycle	t_{SCYC}	SCL	250			ns
SCL H pulse width	t_{SHW}	SCL	100			ns
SCL L pulse width	t_{SLW}	SCL	100			ns
Address setup time	t_{SAS}	A0	150			ns
Address hold time	t_{SAH}	A0	150			ns
Data setup time	t_{SDS}	SI	100			ns
Data hold time	t_{SDH}	SI	100			ns
CS-SCL time	t_{CSS}	/CS1,CS2	150			ns
	t_{CSH}	/CS1,CS2	150			ns

Note The TYP. value is a reference value when $T_A = 25$ °C

(V_{DD} = 2.4 to 2.7 V)

Parameter	Symbol	Conditions	MIN.	TYP. ^{Note}	MAX.	Unit
Shift clock cycle	t _{SCYC}	SCL	400			ns
SCL H pulse width	t _{SHW}	SCL	150			ns
SCL L pulse width	t _{SLW}	SCL	150			ns
Address setup time	t _{SAS}	A0	250			ns
Address hold time	t _{SAH}	A0	250			ns
Data setup time	t _{SDS}	SI	150			ns
Data hold time	t _{SDH}	SI	150			ns
CS-SCL time	t _{CSS}	/CS1,CS2	250			ns
	t _{CSH}	/CS1,CS2	250			ns

Note The TYP. value is a reference value when T_A = 25 °C

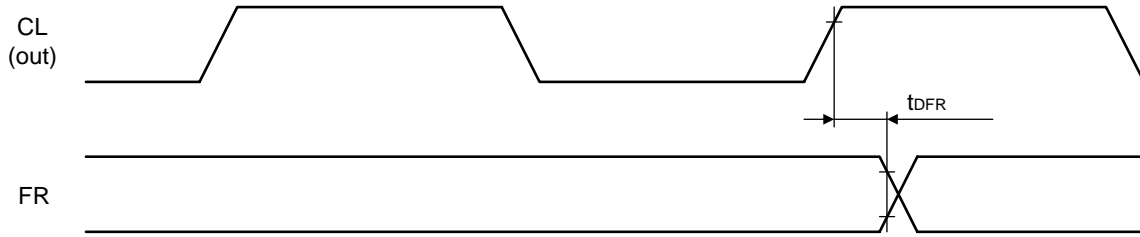
- Remarks**
1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less.
 2. All timing is rated based on 20 % or 80 % of V_{DD}.

Common

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock frequency	f _{CL}	CL, When using external input, V _{DD} = V _{DD2} = 3.0 V ± 10 %, T _A = 25 °C	17	22	25	kHz

- Remarks**
1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less.
 2. The frame time can be determined using the following equation.
 1 frame = 1/f_{osc} or 1/f_{CL} x 4 x duty value
 Therefore, when f_{osc} and f_{CL} = 22 kHz and the duty value is 1/65:
 1 frame = 45.5 μs x 4 x 65 = 11.8 ms (approximately 84.6 Hz)

Output timing for display output control



($V_{DD} = 2.7$ to 4.5 V)

Parameter	Symbol	Conditions	MIN.	TYP. ^{Note}	MAX.	Unit
FR delay time	t_{DFR}	FR, $C_L = 50$ pF		20	80	ns

Note The TYP. value is a reference value when $T_A = 25$ °C

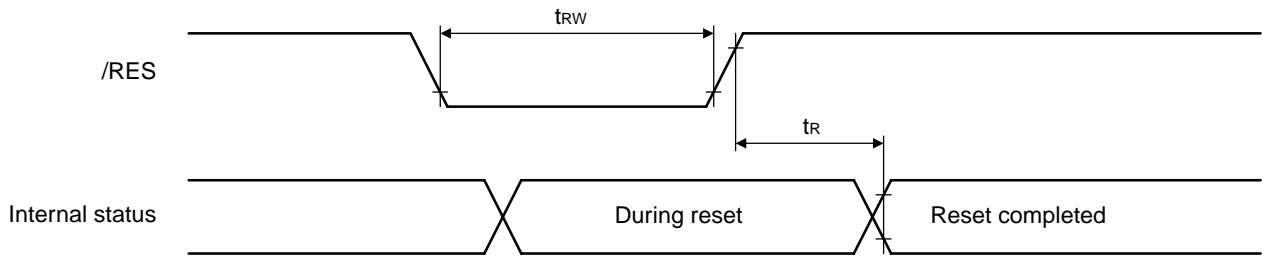
($V_{DD} = 2.4$ to 2.7 V)

Parameter	Symbol	Conditions	MIN.	TYP. ^{Note}	MAX.	Unit
FR delay time	t_{DFR}	FR, $C_L = 50$ pF		50	200	ns

Note The TYP. value is a reference value when $T_A = 25$ °C

Remark All timing is rated based on 20 % or 80 % of V_{DD} .

Reset input timing



($V_{DD} = 2.7$ to 4.5 V)

Parameter	Symbol	Conditions	MIN.	TYP. ^{Note}	MAX.	Unit
Reset time	t_R				1.0	μ s
Reset L pulse width	t_{RW}	$\overline{\text{RES}}$	1.0			μ s

Note The TYP. value is a reference value when $T_A = 25$ °C

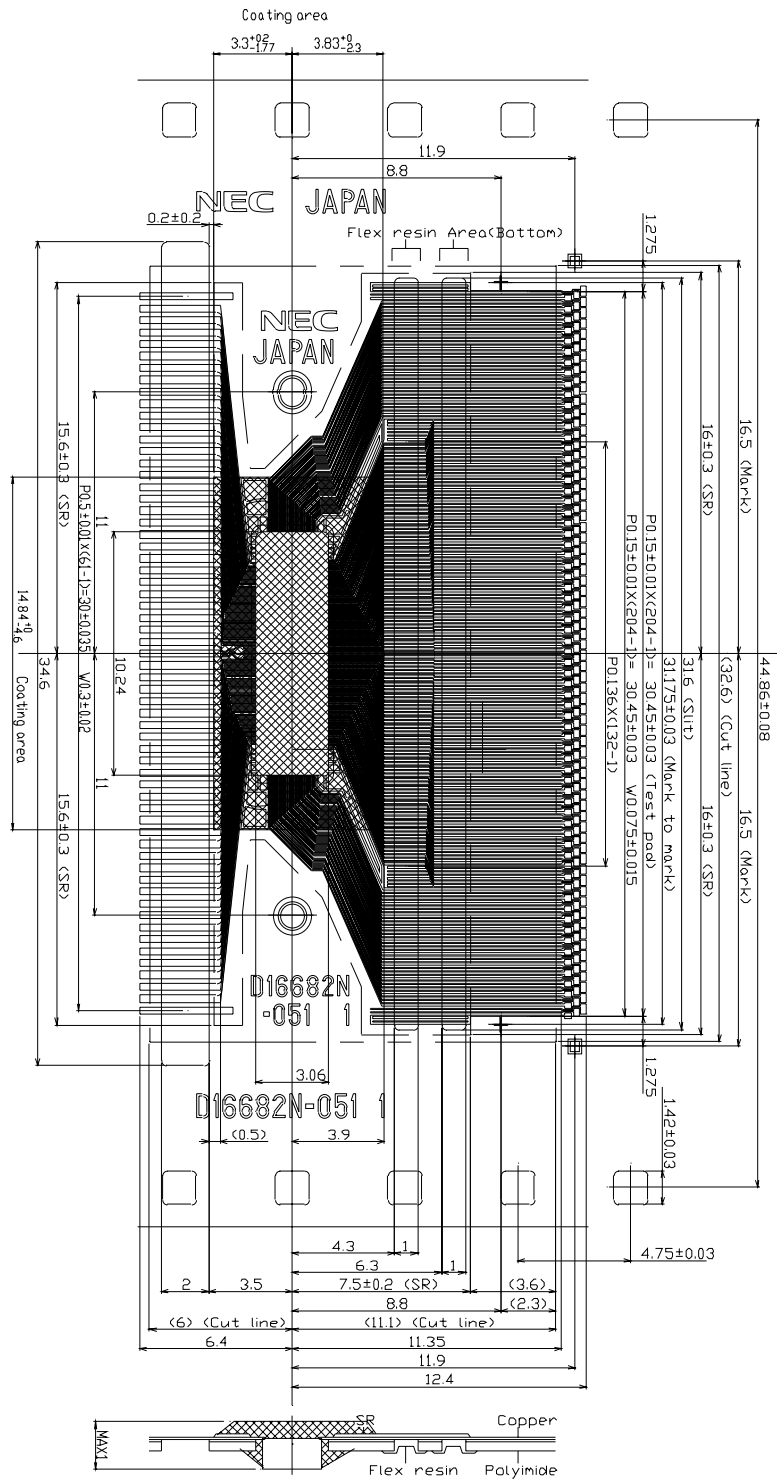
($V_{DD} = 2.4$ to 2.7 V)

Parameter	Symbol	Conditions	MIN.	TYP. ^{Note}	MAX.	Unit
Reset time	t_R				1.5	μ s
Reset L pulse width	t_{RW}	$\overline{\text{RES}}$	1.5			μ s

Note The TYP. value is a reference value when $T_A = 25$ °C

Remark All timing is rated based on 20 % or 80 % of V_{DD} .

15. STANDARD TCP PACKAGE DRAWING (μ PD16682N-xxx-051)(1/3)



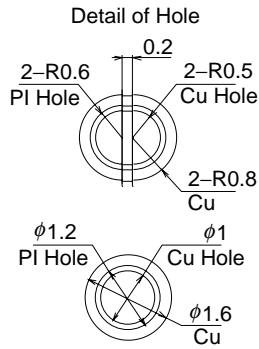
Specification

Polyimide	UPLEX-S	75 μm
Adhesive	Epoxy	12 μm
Copper	Electrolysis Cu	18 μm
Plating	Sn	MIN0.15 μm
Solder Resist	Urethane	20 μm
Backside flex resin	Polyimide	
Coating resin	Epoxy	

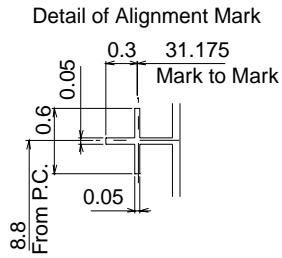
This products is faceup urethane Flex resin type.
 This Figure is shown by Copper side
 over polyimide
 4Sprocket holes(19 mm)
 for 1 Pattern.
 Corner radius is 0.30 mm Max.
 All tolerances unless otherwise
 specified 0.05 mm.

STANDARD TCP PACKAGE DRAWING (μ PD16682N-xxx-051)(2/3)

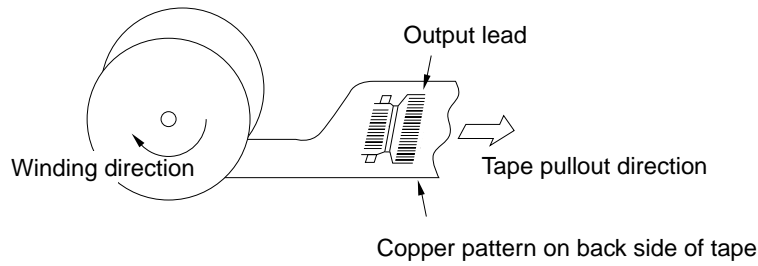
Detail of hole



Detail of alignment mark

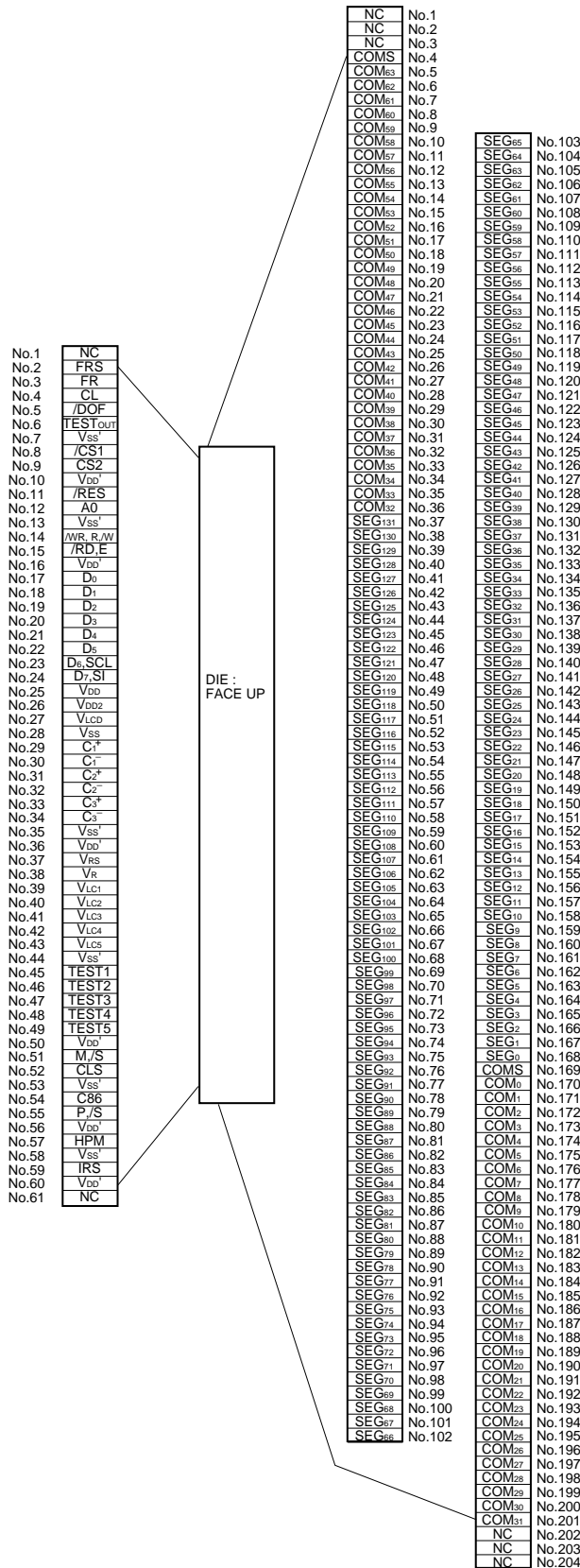


TCP tape winding method



STANDARD TCP PACKAGE DRAWING (μ PD16682N-xxx-051)(3/3)

★ Pin configuration



NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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