

2660 PIXELS CCD LINEAR IMAGE SENSOR

The μ PD3734A is a high sensitivity CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The μ PD3734A has 2660 pixels and an output amplifier which has high gain and wide output range, but low noise.

And it has reset feed-through level clamp circuit, sample and hold circuit and voltage amplifier. Therefore, it is suitable for image scanners, facsimiles and so on.

FEATURES

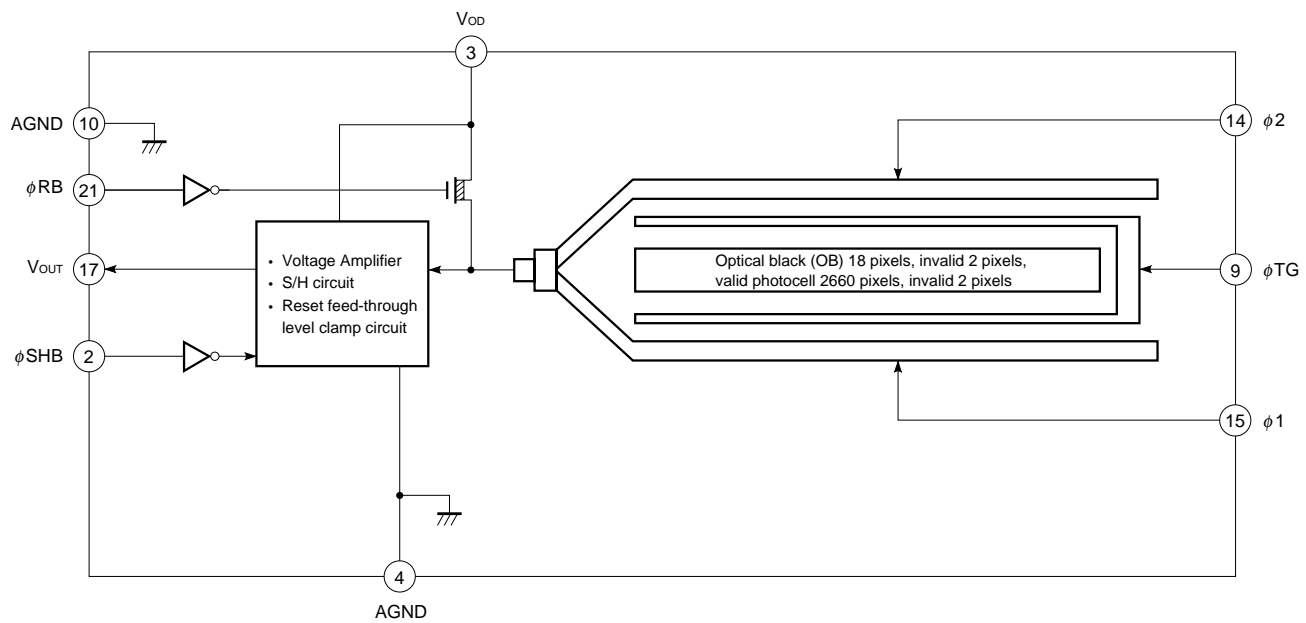
- Valid photocell : 2660 pixels
- Photocell's pitch : 11 μ m
- High sensitivity : 70 V/lx-s TYP.
- Peak response wavelength : 550 nm (green)
- Resolution : 12 dot/mm A4 (210 \times 297 mm) size (shorter side)
300 dpi US letter (8.5" \times 11") size (shorter side)
- Power supply : +12 V
- Drive clock level : CMOS output under 5 V operation
- High speed scan : 0.54 ms/line (S/H in used)
- Built-in circuit : Sample and hold circuit
Reset feed-through level clamp circuit
Clamp pulse generation circuit
Voltage amplifier
- Low noise
- Low image lag : 1 % MAX.

ORDERING INFORMATION

Part Number	Package
μ PD3734ACY	CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

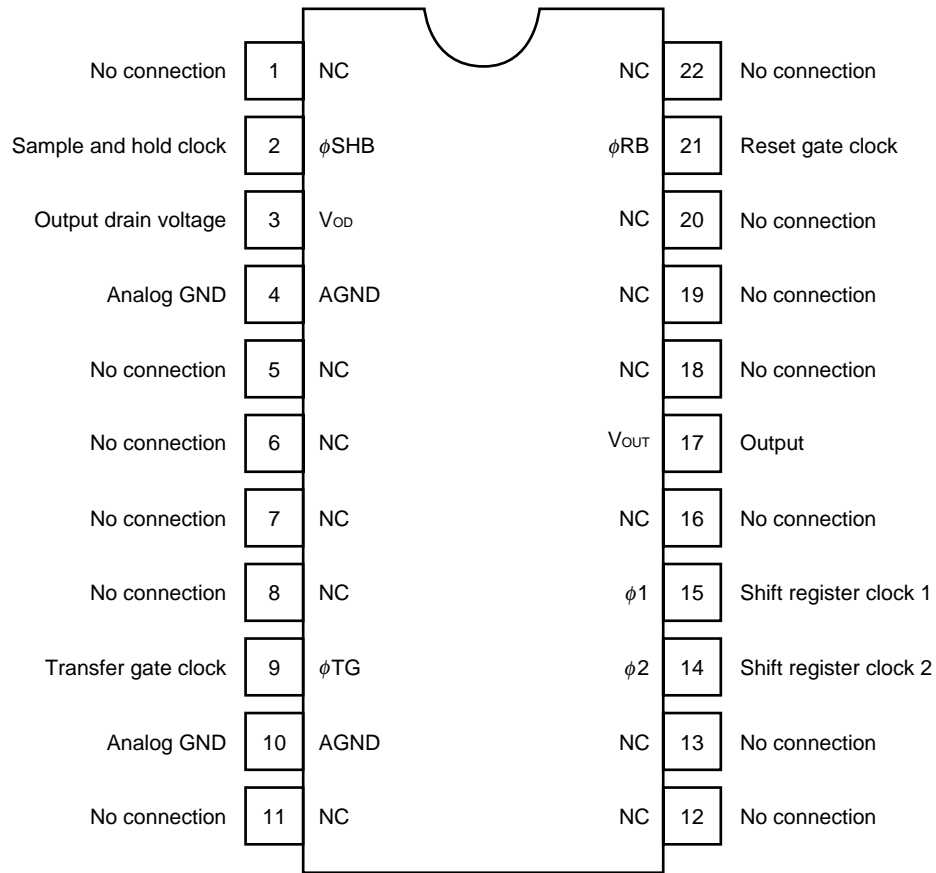
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

BLOCK DIAGRAM



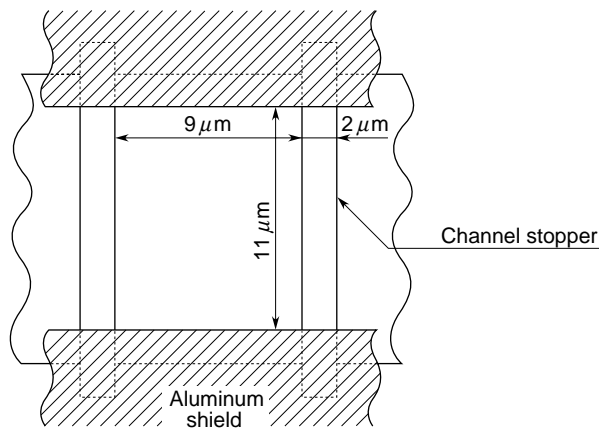
PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))



Caution Connect the No connection pins (NC) to GND.

PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V _{OD}	-0.3 to +15	V
Shift register clock voltage	V _{φ1} , V _{φ2}	-0.3 to +15	V
Reset gate clock voltage	V _{φRB}	-0.3 to +15	V
Transfer gate clock voltage	V _{φTG}	-0.3 to +15	V
Sample and hold clock voltage	V _{φSHB}	-0.3 to +15	V
Operating ambient temperature ^{Note}	T _A	-25 to +60	°C
Storage temperature	T _{stg}	-40 to +70	°C

Note Use at the condition without dew condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output drain voltage	V _{OD}		11.4	12.0	12.6	V
Shift register clock high level	V _{φ1H} , V _{φ2H}		4.5	5.0	5.5	V
Shift register clock low level	V _{φ1L} , V _{φ2L}		-0.3	0	+0.5	V
Reset gate clock high level	V _{φRBH}		4.5	5.0	5.5	V
Reset gate clock low level	V _{φRBL}		-0.3	0	+0.5	V
Transfer gate clock high level	V _{φTGH}		4.5	5.0	5.5	V
Transfer gate clock low level	V _{φTGL}		-0.3	0	+0.5	V
Sample and hold clock high level	V _{φSHBH}		4.5	5.0	5.5	V
Sample and hold clock low level	V _{φSHBL}		-0.3	0	+0.5	V
Data rate	f _{φRB}	S/H in used	0.2	1	5	MHz
		S/H not in used	0.2	1	4	MHz

ELECTRICAL CHARACTERISTICS

($T_A = +25^{\circ}\text{C}$, $V_{OD} = 12\text{ V}$, $f_{\phi 1} = 0.5\text{ MHz}$, data rate = 1 MHz, storage time = 10 ms
light source: 3200 K halogen lamp + C-500S (infrared cut filter, $t = 1\text{ mm}$), input signal clock = 5 V_{p-p})

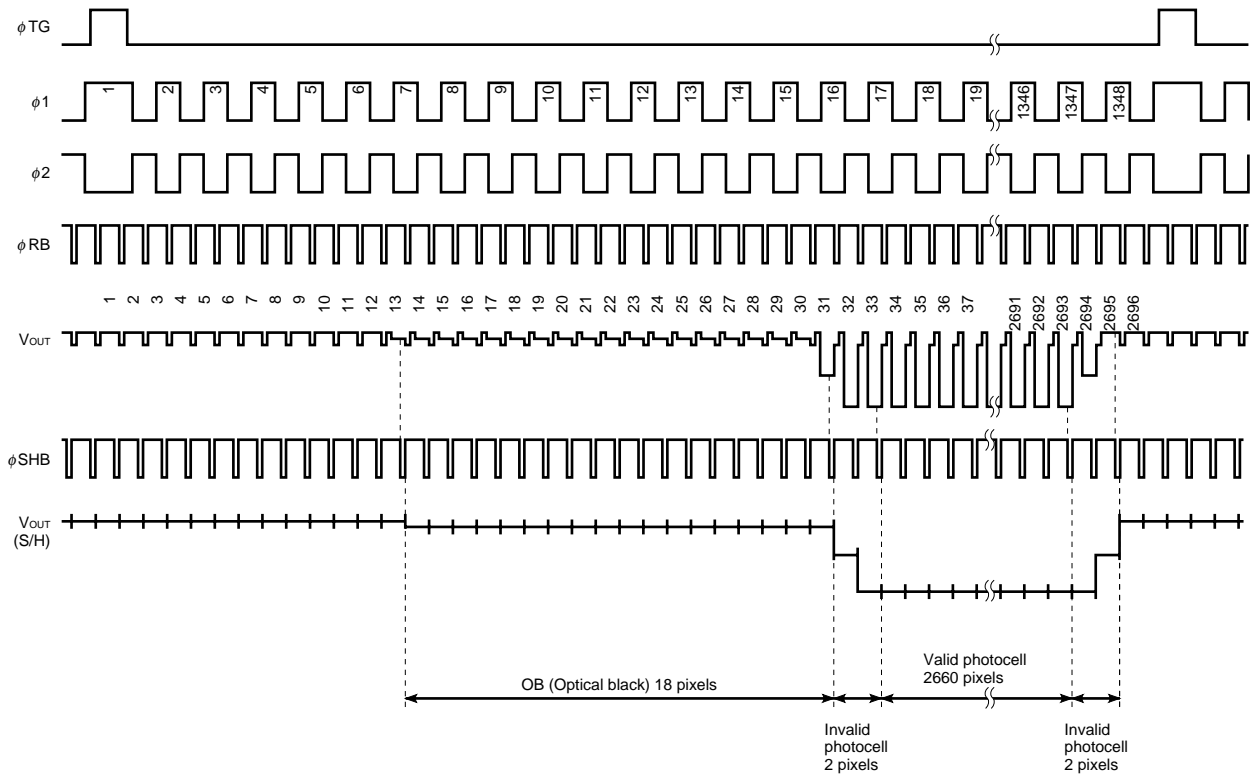
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{sat}		1.5	2.0	–	V
Saturation exposure	SE	Daylight color fluorescent lamp	–	0.029	–	$\text{lx}\cdot\text{s}$
Photo response non-uniformity	PRNU	$V_{OUT} = 500\text{ mV}$	–	± 2	± 8	%
Average dark signal	ADS	Light shielding	–	1.0	3.0	mV
Dark signal non-uniformity	DSNU	Light shielding	–	4	6	mV
Power consumption	P_w		–	190	250	mW
Output impedance	Z_o		–	0.5	1	$\text{k}\Omega$
Response	R_F	Daylight color fluorescent lamp	49	70	91	$\text{V}/\text{lx}\cdot\text{s}$
Response peak			–	550	–	nm
Image lag	IL	$V_{OUT} = 1\text{ V}$	–	0.3	1.0	%
Offset level	V_{OS}		3.5	4.5	5.5	V
★ Output fall delay time ^{Note}	t_d	$V_{OUT} = 500\text{ mV}$, $t_1, t_2 = 30\text{ ns}$	–	80	–	ns
Register imbalance	RI	$V_{OUT} = 500\text{ mV}$	0	–	3	%
Total transfer efficiency	TTE	$V_{OUT} = 1\text{ V}$, data rate = 4 MHz	92	–	–	%
Dynamic range	DR	V_{sat}/DSNU	–	500	–	times
Reset feed-through noise	RFSN	Light shielding	–900	–200	+500	mV
Sample and hold noise	SHSN	Light shielding, ϕSHB series resistor $47\ \Omega$	–50	0	+50	mV
Bit noise	BN		–	4.5	–	mV_{p-p}
Random noise	σ	S/H in used	–	0.9	–	mV
		S/H not in used	–	0.9	–	mV
Resolution	MTF	Modulation transfer function at nyquist frequency	–	65	–	%

Note Refer to TIMING CHART2.

★ INPUT PIN CAPACITANCE ($T_A = +25^\circ\text{C}$, $V_{OD} = 12\text{ V}$)

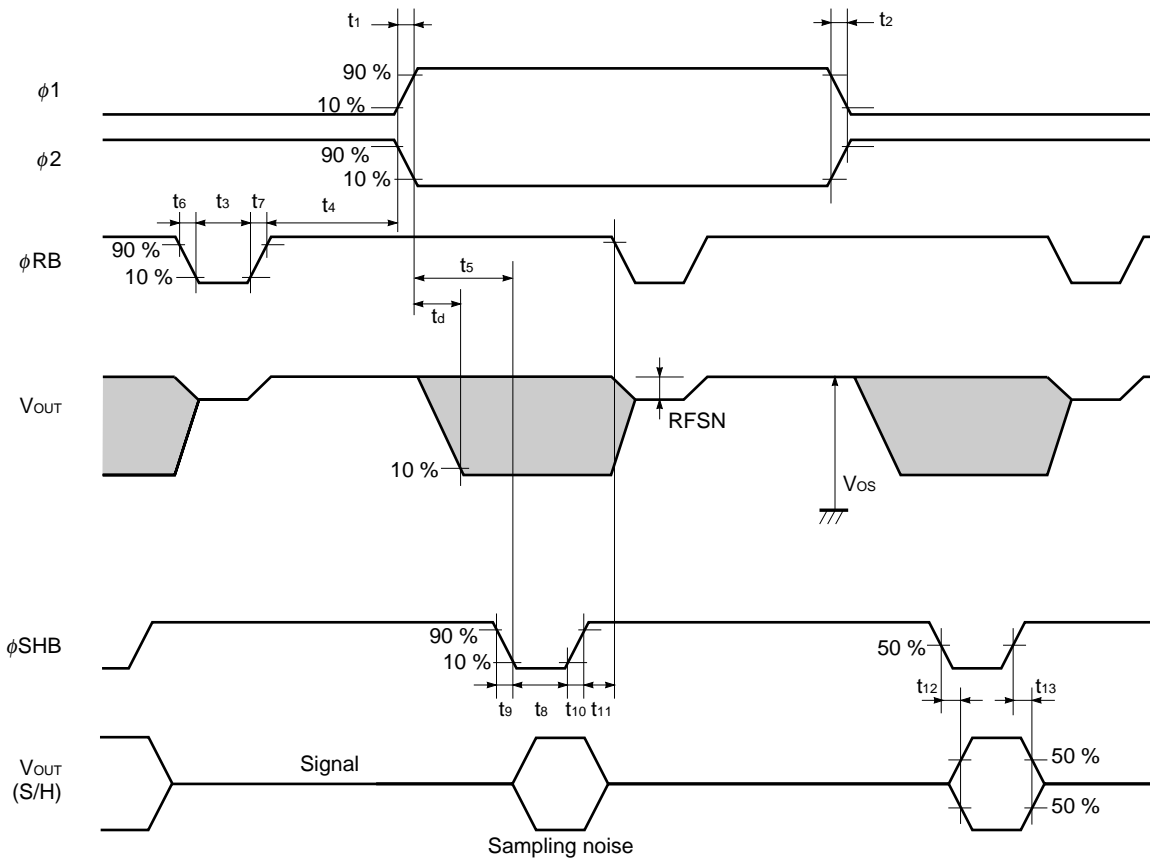
Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	$\phi 1$	15	–	400	–	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	$\phi 2$	14	–	400	–	pF
Sample and hold clock pin capacitance	$C_{\phi\text{SHB}}$	ϕSHB	2	–	5	–	pF
Reset gate clock pin capacitance	$C_{\phi\text{RB}}$	ϕRB	21	–	5	–	pF
Transfer gate clock pin capacitance	$C_{\phi\text{TG}}$	ϕTG	9	–	100	–	pF

TIMING CHART 1



Remark V_{out} = Output when ϕ_{SHB} is not in used (When ϕ_{SHB} is not in used, connect ϕ_{SHB} pin to GND).
 $V_{out} (S/H)$ = Output when ϕ_{SHB} is in used.

TIMING CHART 2



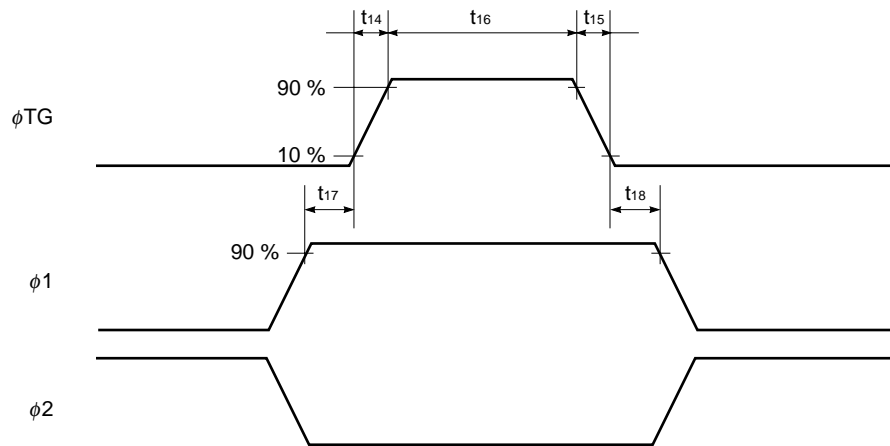
Remark $V_{out}(S/H)$ = Output when ϕSHB is in used.

★

Parameter	MIN.	TYP.	MAX.	Unit
t_1, t_2	0	50	(100)	ns
t_3	20	100	—	ns
t_4	90	300	—	ns
t_5	70	300	—	ns
t_6, t_7	0	50	—	ns
t_8	20	200	—	ns
t_9, t_{10}, t_{11}	0	50	—	ns
t_{12}	0	—	—	ns
t_{13}	—	5	10	ns

Remark The MAX. in the table above shows the operation range in which the output characteristics are kept almost enough for general purpose, does not show the limit above which the μPD3734A is destroyed.

TIMING CHART for φTG, φ1, φ2

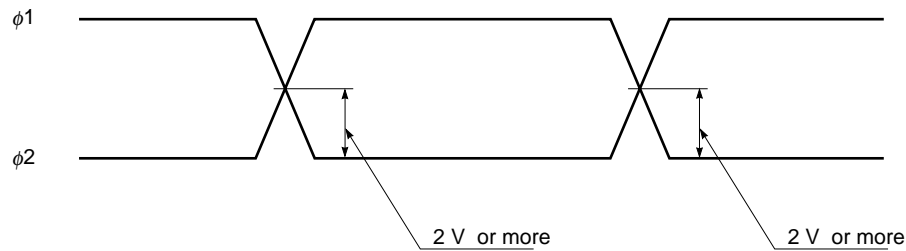


★

Parameter	MIN.	TYP.	MAX.	Unit
t14, t15	0	50	–	ns
t16	650	1000	(2000)	ns
t17, t18	0	100	–	ns

Remark The MAX. in the table above shows the operation range in which the output characteristics are kept almost enough for general purpose, does not show the limit above which the μPD3734A is destroyed.

CROSS POINTS for φ1, φ2



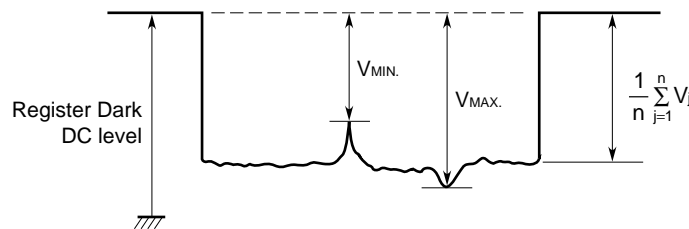
Remark Adjust cross point of φ1, φ2 by φ1, φ2 pin external input resistors.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: V_{sat}
Output signal voltage at which the response linearity is lost.
2. Saturation exposure: SE
Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.
3. Photo response non-uniformity: PRNU
The peak/bottom ratio to the average output voltage of all the valid pixels calculated by the following formula.

$$PRNU (\%) = \left(\frac{V_{MAX. \text{ or } V_{MIN.}}}{\frac{1}{n} \sum_{j=1}^n V_j} - 1 \right) \times 100$$

n : Number of valid pixels
 V_j : Output voltage of each pixel



4. Average dark signal: ADS
Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

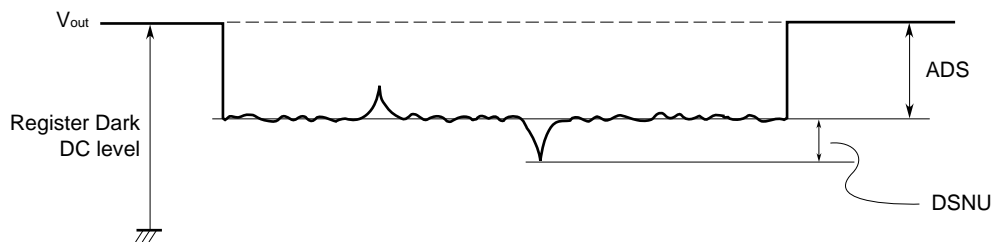
$$ADS (mV) = \frac{\sum_{j=1}^{2660} d_j}{2660}$$

d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity: DSNU
Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

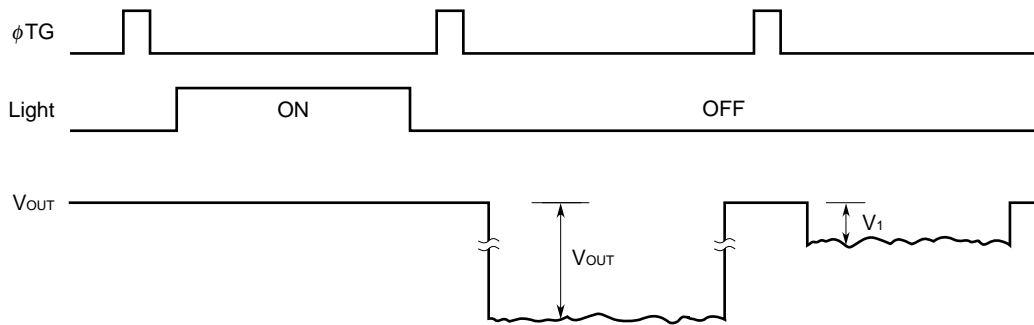
$$DSNU (mV): \text{maximum of } |d_j - ADS| \text{ } j = 1 \text{ to } 2660$$

d_j : Dark signal of valid pixel number j



- 6. Output impedance: Z_o
Output pin impedance viewed from outside.
- 7. Response: R
Output voltage divided by exposure (lx·s).
Note that the response varies with a light source (spectral characteristic).

- 8. Image Lag: IL
The rate between the last output voltage and the next one after read out the data of a line.



$$IL (\%) = \frac{V_1}{V_{OUT}} \times 100$$

- 9. Register Imbalance: RI
The rate of the difference between the average of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

n : Number of valid pixels
V_j : Output voltage of each pixel

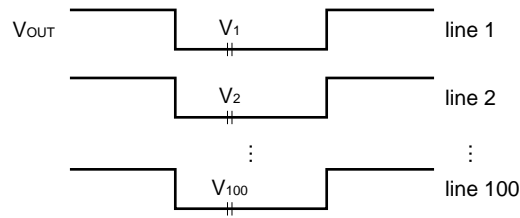
- 10. Bit Noise: BN
Output signal distribution of a photocell by scan.

11. Random noise: σ

Random noise σ is defined as the standard deviation of a valid photocell output signal with 100 times (= 100 lines) data sampling at dark (light shielding).

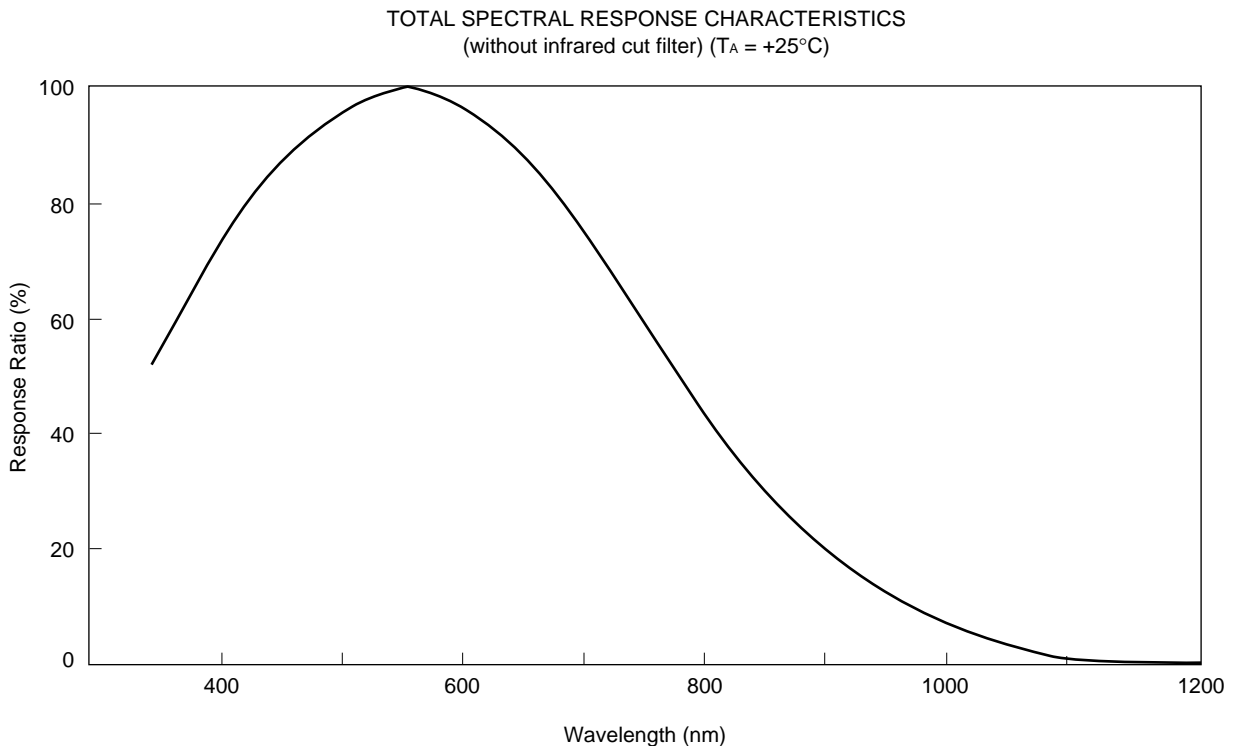
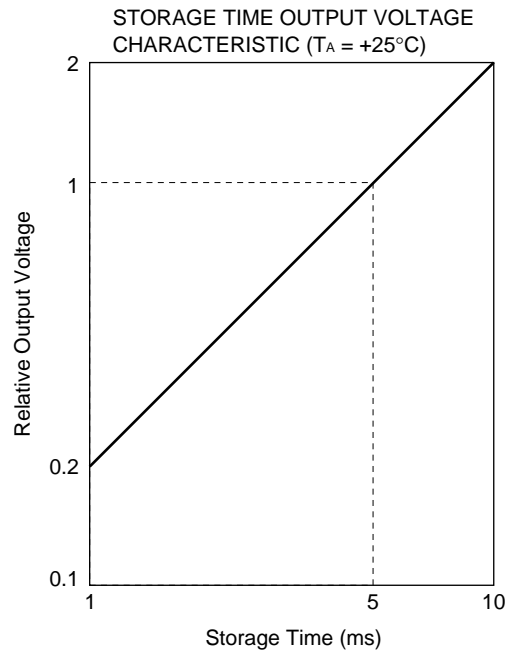
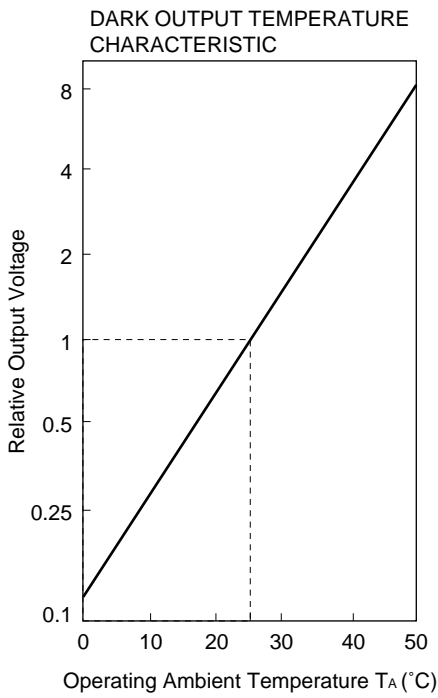
$$\sigma \text{ (mV)} = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

V_i : A valid photocell output signal among all of the valid photocells

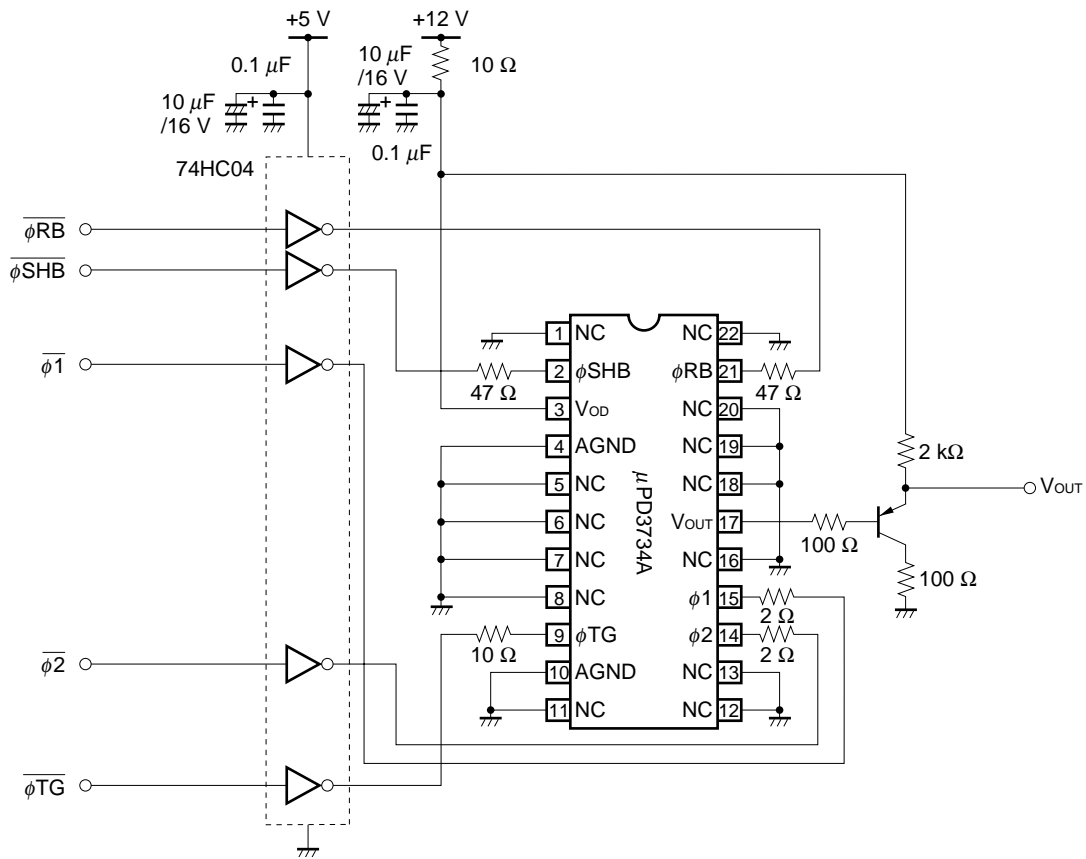


This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

STANDARD CHARACTERISTIC CURVES (Reference Value)



APPLICATION CIRCUIT EXAMPLE



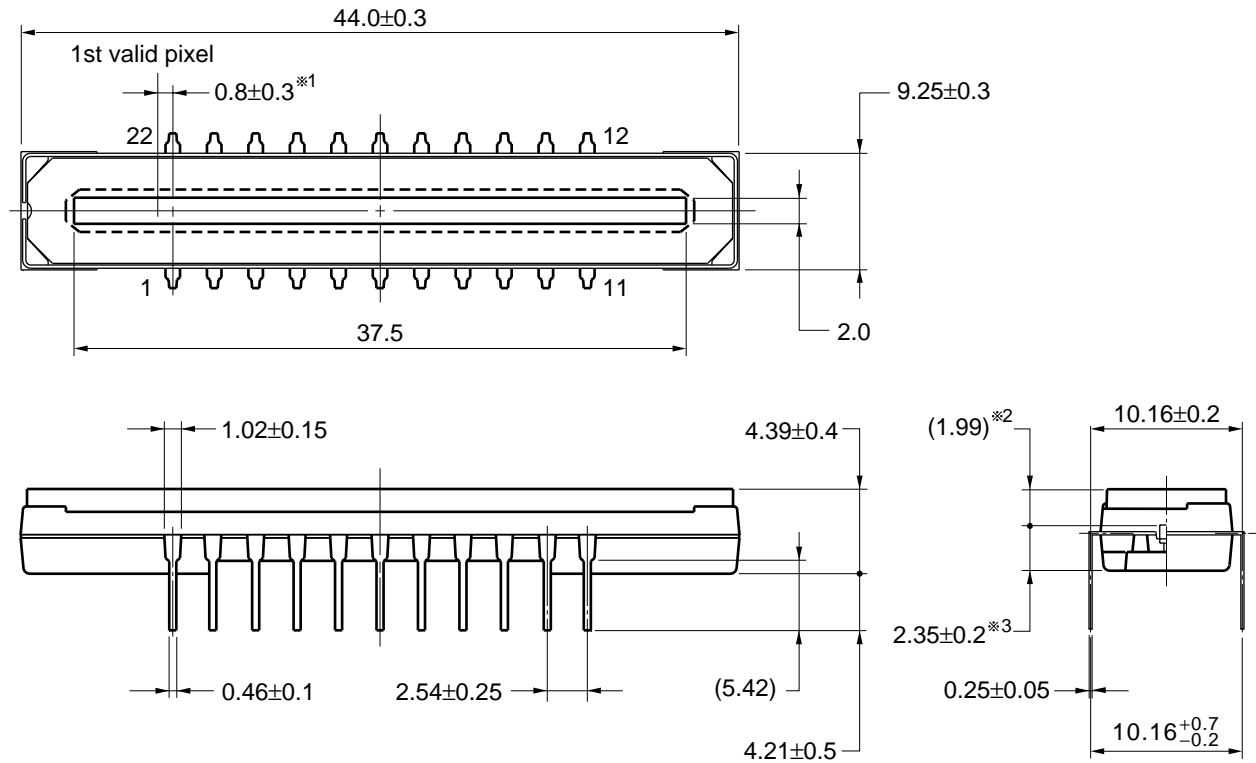
Caution Connect the No connection pins (NC) to GND.

Remark When internal sample and hold circuit of the μPD3734A is not necessary, connect pin 2 (φSHB) to GND.

★ PACKAGE DIMENSIONS

μPD3734ACY
 CCD LINEAR IMAGE SENSOR 22-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	42.9×8.35×0.7	1.5

- ※1 1st valid pixel ←→ The center of the pin1
- ※2 The surface of the CCD chip ←→ The top of the cap
- ※3 The bottom of the package ←→ The surface of the CCD chip

22C-1CCD-PKG16-1

★ RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD3734ACY: CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (per each lead).

- Cautions**
1. During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.
 2. Soldering by the solder flow method may have deleterious effects on prevention of plastic cap soiling and heat resistance. So the method cannot be guaranteed.

★

NOTES ON HANDLING THE PACKAGES

① DUST AND DIRT PROTECTING

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning. Don't either touch plastic cap surface by hand or have any object come in contact with plastic cap surface. Should dirt stick to a plastic cap surface, blow it off with an air blower. For dirt stuck through electricity ionized air is recommended. And if the plastic cap surface is grease stained, clean with our recommended solvents.

○ CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.
We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

○ RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap.
Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

② MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with plastic cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers or of pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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