NEC

MOS INTEGRATED CIRCUIT

μPD789405A, 789406A, 789407A, 789415A, 789416A, 789417A

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD789405A, 789406A, 789407A, 789415A, 789416A, and 789417A are products of the μPD789407A and 789417A Subseries (for LCD drive) in the 78K/0S Series.

In addition, a flash memory version (μPD78F9418A) that can operate within the same power-supply voltage range as the mask ROM version, and a range of development tools are also supported.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789407A, 789417A Subseries User's Manual: U13952E
78K/0S Series User's Manual Instructions: U11047E

FEATURES

- **ROM and RAM sizes**

Part Number \ Item	Program Memory (ROM)	Data Memory	
		Internal High-Speed RAM	LCD Display RAM
★ μPD789405A, 789415A	12 KB	512 × 8 bits	28 × 4 bits
μPD789406A, 789416A	16 KB		
μPD789407A, 789417A	24 KB		

- Minimum instruction execution time can be changed from high-speed (0.4 μs @ 5.0 MHz operation with main system clock) to ultra-low-speed (122 μs @ 32.768 kHz operation with subsystem clock)
- I/O ports: 43
- Serial interface: 1 channel
  3-wire serial I/O mode/UART mode selectable
- LCD controller/driver
  - Segment signals: 28 MAX.
  - Common signals: 4 MAX.
  - 1/2- or 1/3-bias selectable
- 8-bit resolution A/D converter: 7 channels (μPD789405A, 789406A, 789407A)
- 10-bit resolution A/D converter: 7 channels (μPD789415A, 789416A, 789417A)
- Timer: 6 channels
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 2 channels
  - 8-bit timer: 1 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- Supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATION FIELDS

APS compact cameras, blood pressure gauges, rice cookers, etc.

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The mark ★ shows major revised points.

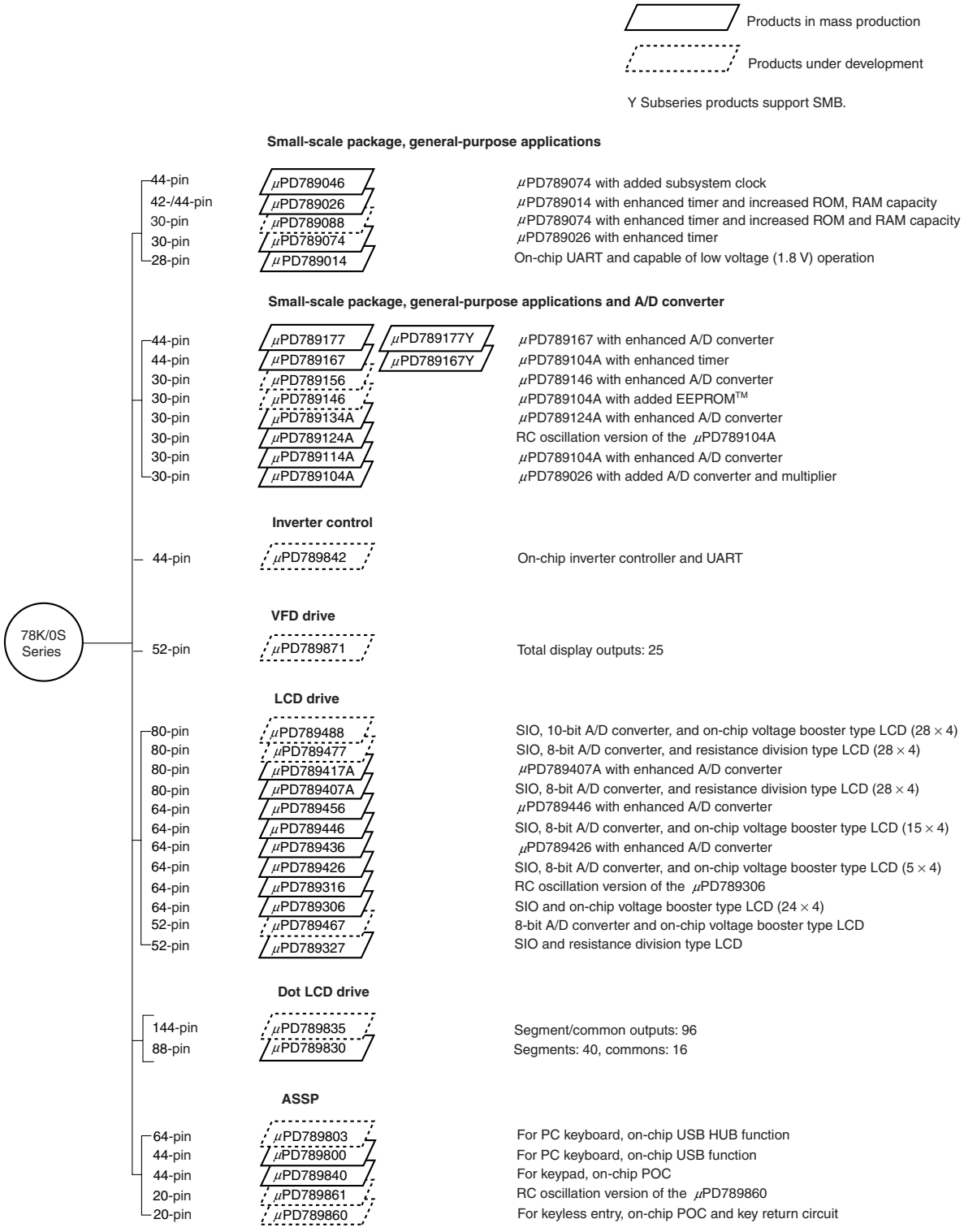
★ ORDERING INFORMATION

Part Number	Package
μPD789405AGC-×××-8BT	80-pin plastic QFP (14 × 14)
μPD789405AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
μPD789406AGC-×××-8BT	80-pin plastic QFP (14 x 14)
μPD789406AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
μPD789407AGC-×××-8BT	80-pin plastic QFP (14 x 14)
μPD789407AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
μPD789415AGC-×××-8BT	80-pin plastic QFP (14 × 14)
μPD789415AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
μPD789416AGC-×××-8BT	80-pin plastic QFP (14 x 14)
μPD789416AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
μPD789417AGC-×××-8BT	80-pin plastic QFP (14 × 14)
μPD789417AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)

Remark ××× indicates ROM code suffix.

DEVELOPMENT OF 78K/0S SERIES

The product development of the 78K/0S Series is shown below. Subseries names are shown enclosed in a solid or dotted line.



Remark VFD (Vacuum Fluorescent Display) is referred to as "FIP™" (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
Small-scale package, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 K to 16 K			–							
	μPD789088	16 K to 32 K	3 ch							24		
	μPD789074	2 K to 8 K	1 ch									
	μPD789014	2 K to 4 K	2 ch	–						22		
Small-scale package, general-purpose applications and A/D converter	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch		–	8 ch	1 ch (UART: 1 ch)	31		–
	μPD789167						8 ch	–				
	μPD789156	8 K to 16 K	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K to 8 K					–	4 ch				RC-oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
VFD drive	μPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
LCD drive	μPD789488	32 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789477	24 K					8 ch	–				
	μPD789417A	12 K to 24 K					–	7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 K to 16 K	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16 K					–		2 ch (UART: 1 ch)	23		RC-oscillation version
	μPD789306											–
	μPD789427	4 K to 24 K		–			1 ch		–	18		
	μPD789327						–		1 ch	21		
Dot LCD drive	μPD789835	24 K to 60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	28	1.8 V	–
	μPD789830	24 K	1 ch	1 ch			–			30	2.7 V	
ASSP	μPD789803	8 K to 16 K	2 ch	–	–	1 ch	–	–	2 ch (USB: 1 ch)	41	3.6 V	–
	μPD789800	8 K								31	4.0 V	
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K					–		–	14	1.8 V	RC-oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM

Note 10-bit timer: 1 channel

FUNCTIONAL OUTLINE

Item		μPD789405A μPD789415A	μPD789406A μPD789416A	μPD789407A μPD789417A
Internal memory	ROM	12 KB	16 KB	24 KB
	High-speed RAM	512 bytes		
★	LCD display RAM	28 × 4 bits		
Minimum instruction execution time		0.4 μs/1.6 μs (@ 5.0 MHz operation with main system clock) 122 μs (@ 32.768 kHz operation with main system clock)		
General-purpose registers		8 bits × 8 registers		
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test), etc.		
I/O ports		Total: 43 • CMOS input: 7 • CMOS I/O: 32 • N-ch open-drain (12 V): 4		
A/D converters		• 8-bit resolution × 7 channels (μPD789405A, 789406A, 789407A) • 10-bit resolution × 7 channels (μPD789415A, 789406A, 789407A)		
Comparator		Timer output controllable		
Serial interface		3-wire serial I/O mode/UART mode selectable: 1 channel		
LCD controller/driver		• Segment signal output: 28 MAX • Common signal output: 4 MAX • 1/2 or 1/3 bias selectable		
Timers		• 16-bit timer: 1 channel • 8-bit timer: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel		
Timer output		2		
Vectored interrupt sources	Maskable	Internal: 12, external: 4		
	Non-maskable	Internal: 1		
Supply voltage		V_{DD} = 1.8 to 5.5 V		
Operating ambient temperature		T_A = –40 to +85°C		
Package		• 80-pin plastic QFP (14 × 14) • 80-pin plastic TQFP (fine pitch) (12 × 12)		

TABLE OF CONTENTS

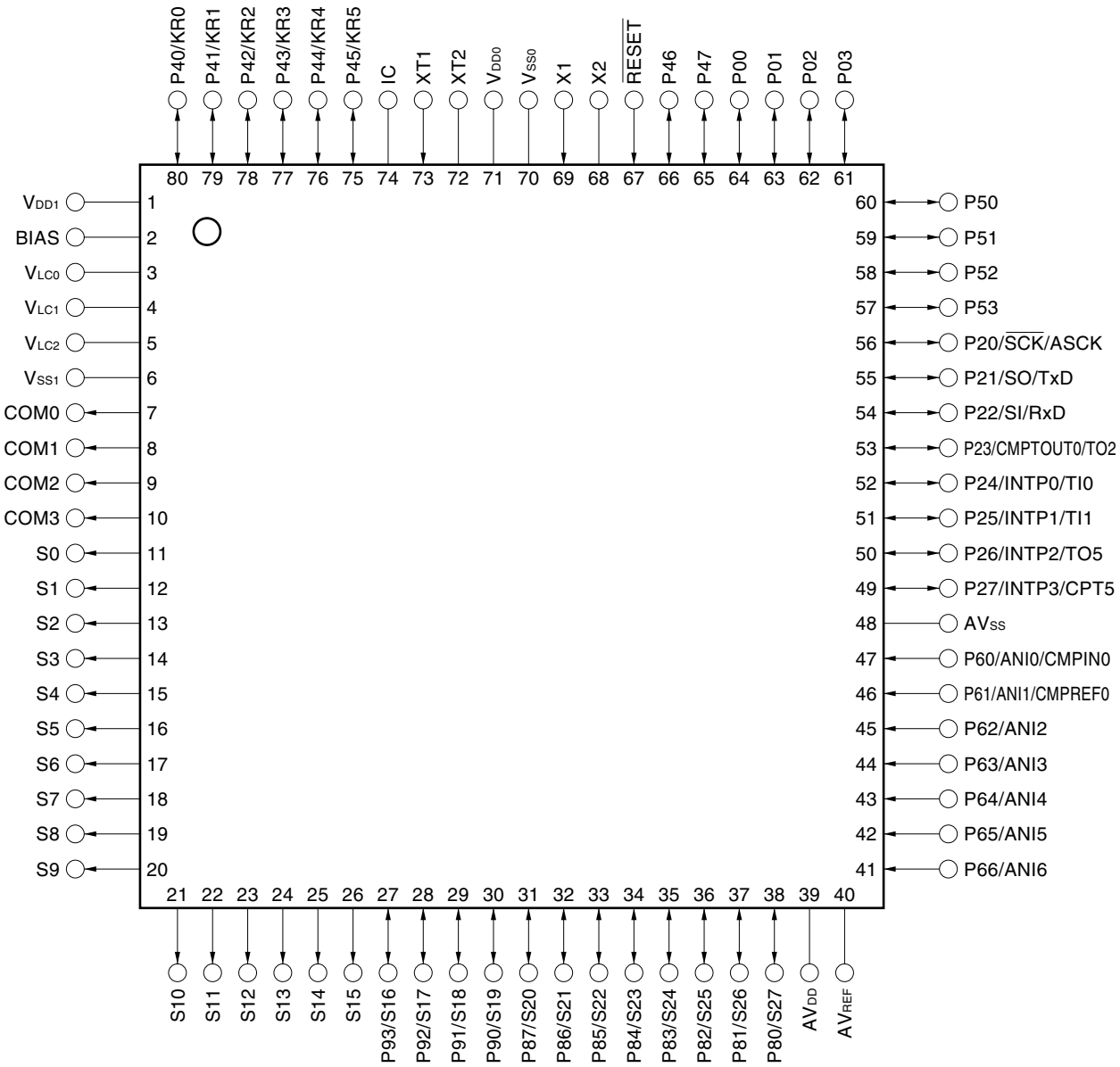
1. PIN CONFIGURATION (TOP VIEW)

• 80-pin plastic QFP (14 x 14)

μPD789405AGC-×××-8BT
μPD789406AGC-×××-8BT
μPD789407AGC-×××-8BT
μPD789415AGC-×××-8BT
μPD789416AGC-×××-8BT
μPD789417AGC-×××-8BT

• 80-pin plastic TQFP (fine pitch) (12 × 12)

μPD789405AGK-×××-9EU
μPD789406AGK-×××-9EU
μPD789407AGK-×××-9EU
μPD789415AGK-×××-9EU
μPD789416AGK-×××-9EU
μPD789417AGK-×××-9EU



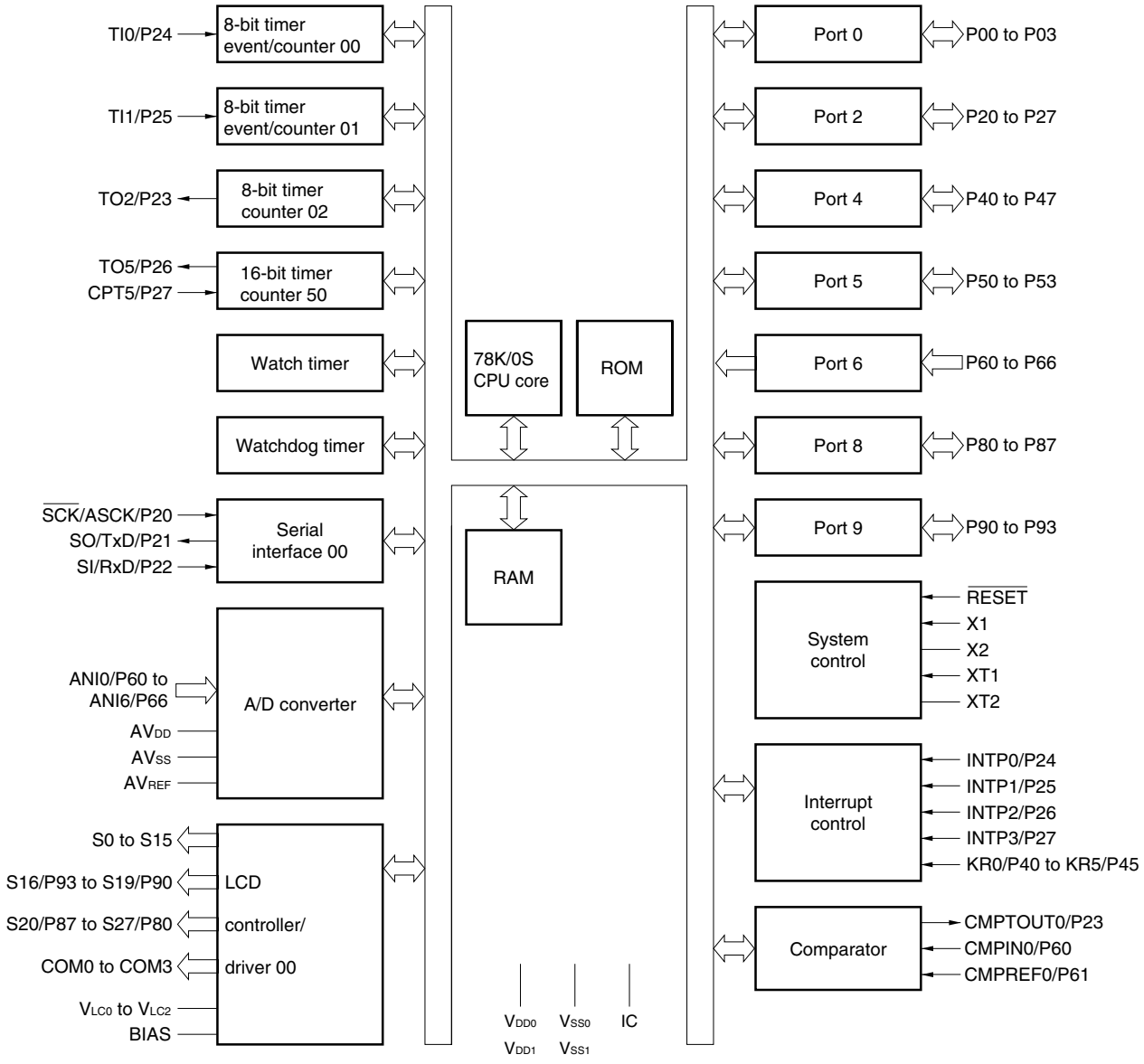
Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

★ **2. Connect the AV_{DD} pin to V_{SS0}.**

★ **3. Connect the AV_{SS} pin to V_{SS0}.**

ANI0 to ANI6:	Analog input
ASCK:	Asynchronous serial input
AV_{DD}:	Analog power supply
AV_{REF}:	Analog reference voltage
AV_{SS}:	Analog ground
BIAS:	LCD power supply bias control
CMPIN0:	Comparator input
CMPREF0:	Comparator reference
CMPTOUT0:	Comparator output
COM0 to COM3:	Common output
CPT5:	Capture trigger input
IC:	Internally connected
INTP0 to INTP3:	External interrupt input
KR0 to KR5:	Key return
P00 to P03:	Port 0
P20 to P27:	Port 2
P40 to P47:	Port 4
P50 to P53:	Port 5
P60 to P66:	Port 6
P80 to P87:	Port 8
P90 to P93:	Port 9
$\overline{\text{RESET}}$:	Reset
RxD:	Receive data
S0 to S27:	Segment output
$\overline{\text{SCK}}$:	Serial clock
SI:	Serial input
SO:	Serial output
TI0, TI1:	Timer input
TO2, TO5:	Timer output
TxD:	Transmit data
V_{DD0}, V_{DD1}:	Power supply
V_{LC0} to V_{LC2}:	LCD power supply
V_{SS0}, V_{SS1}:	Ground
X1, X2:	Crystal (main system clock)
XT1, XT2:	Crystal (subsystem clock)

★ 2. BLOCK DIAGRAM



Remark The internal ROM capacity differs depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as input port, an on-chip pull-up resistor can be specified via software.	Input	–
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as input port, an on-chip pull-up resistor can be specified via software.	Input	$\overline{\text{SCK}}$/ASCK
P21				SO/TxD
P22				SI/RxD
P23				CMPTOUT0/TO2
P24				INTP0/TI0
P25				INTP1/TI1
P26				INTP1/TO5
P27				INTP3/CPT5
P40 to P45	I/O	Port 4. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as input port, an on-chip pull-up resistor can be specified via software.	Input	KR0 to KR5
P46, P47				–
P50 to P53	I/O	Port 5. 4-bit N-ch open-drain I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by mask option.	Input	–
P60	Input	Port 6. 7-bit input-only port.	Input	ANI0/CMPIN0
P61				ANI1/CMPREF0
P62 to P66				ANI2 to ANI6
P80 to P87	I/O	Port 8. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as input port, an on-chip pull-up resistor can be specified via software.	Input	S27 to S20
P90 to P93	I/O	Port 9. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as input port, an on-chip pull-up resistor can be specified via software.	Input	S19 to S16

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P24/TI0
INTP1				P25/TI1
INTP2				P26/TO5
INTP3				P27/CPT5
KR0 to KR5	Input	Key return signal detection	Input	P40 to P45
SI	Input	Serial data input to serial interface	Input	P22/RxD
SO	Output	Serial data output from serial interface	Input	P21/TxD
$\overline{SCK}$	I/O	Serial clock input/output for serial interface	Input	P20/ASCK
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{SCK}$
RxD	Input	Serial data input for asynchronous serial interface	Input	P22/SI
TxD	Output	Serial data output for asynchronous serial interface	Input	P21/SO
TI0	Input	External count clock input to 8-bit timer (TM00)	Input	P24/INTP0
TI1	Input	External count clock input to 8-bit timer (TM01)	Input	P25/INTP1
TO2	Output	8-bit timer (TM02) output	Input	P23/CMPTOUT0
TO5	Output	16-bit timer (TM50) output	Input	P26/INTP2
CPT5	Input	Capture edge input	Input	P27/INTP3
CMPTOUT0	Output	Comparator output	Input	P23/TO2
CMPIN0	Input	Comparator input	Input	P60/ANI0
CMPREF0	Input	Comparator reference voltage input	Input	P61/ANI1
ANI0	Input	A/D converter analog input	Input	P60/CMPIN0
ANI1				P61/CMPREF0
ANI2 to ANI6				P62 to P66
AV_{REF}	–	A/D converter reference voltage	–	–
AV_{SS}	–	A/D converter ground potential	–	–
AV_{DD}	–	A/D converter analog power supply	–	–
S0 to S15	Output	Segment signal output from LCD controller/driver	Output	–
S16 to S19			Input	P93 to P90
S20 to S27				P87 to P80
COM0 to COM3	Output	Common signal output from LCD controller/driver	Output	–
V_{LC0} to V_{LC2}	–	LCD drive voltage	–	–
BIAS	–	Supply voltage for LCD driving	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{RESET}$	Input	System reset input	Input	–

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
V_{DD0}	–	Positive power supply	–	–
V_{DD1}	–	Positive power supply (other than ports)	–	–
V_{SS0}	–	Ground	–	–
V_{SS1}	–	Ground potential (other than ports)	–	–
IC	–	Internally connected. Connect this pin directly to V_{SS0} or V_{SS1}.	–	–

3.3 Pin I/O Circuits and Recommended Connections of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins in shown in Table 3-1.
For the I/O circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin I/O Circuits and Recommended Connections of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00 to P03	5-H	I/O	Input: Independently connect to V_{DD0}, V_{DD1} or V_{SS0}, V_{SS1} via a resistor.
P20/$\overline{SCK}$/ASCK	8-C		Output: Leave open.
P21/SO/TxD			
P22/SI/RxD			
P23/CMPTOUT0/TO2	10-B		
★ P24/INTP0/TI0	8-C		Input: Independently connect to V_{SS0} or V_{SS1}, V_{SS1} via a resistor.
★ P25/INTP1/TI1			Output: Leave open.
★ P26/INTP2/TO5			
★ P27/INTP3/CPT5			
P40/KR0 to P45/KR5			Input: Independently connect to V_{DD0}, V_{DD1} or V_{SS0}, V_{SS1} via a resistor.
P46, P47	5-H		Output: Leave open.
P50-P53	13-U		Input: Independently connect to V_{DD0} or V_{DD1} via a resistor.
			Output: Leave open.
P60/ANI0/CMPIN0	9-D	Input	Connect directly to V_{DD0}, V_{DD1} or V_{SS0}, V_{SS1}.
P61/ANI1/CMPREF0			
P62/ANI2 to P66/ANI6	9-C		
P80/S27 to P87/S20	17-F	I/O	Input : Independently connect to V_{DD0}, V_{DD1} or V_{SS0}, V_{SS1} via a resistor.
P90/S19 to P93/S16			Output : Leave open.
S0 to S15	17-B	Output	Leave open.
COM0 to COM3	18-A		
V_{LC0} to V_{LC2}	–	–	
BIAS			Leave open (If all V_{LC0} to V_{LC2} are unused, however, independently connect them to V_{SS0} or V_{SS1} via resistor).
XT1		Input	Connect to V_{SS0} or V_{SS1}.
XT2		–	Leave open.
★ AV_{DD}			Connect to V_{DD0}
★ AV_{SS}			Connect to V_{SS0}
★ AV_{REF}			Connect to V_{DD0}
$\overline{RESET}$	2	Input	–
IC	–	–	Connect directly to V_{SS0} or V_{SS1}.

Figure 3-1. Pin I/O Circuits (1/2)

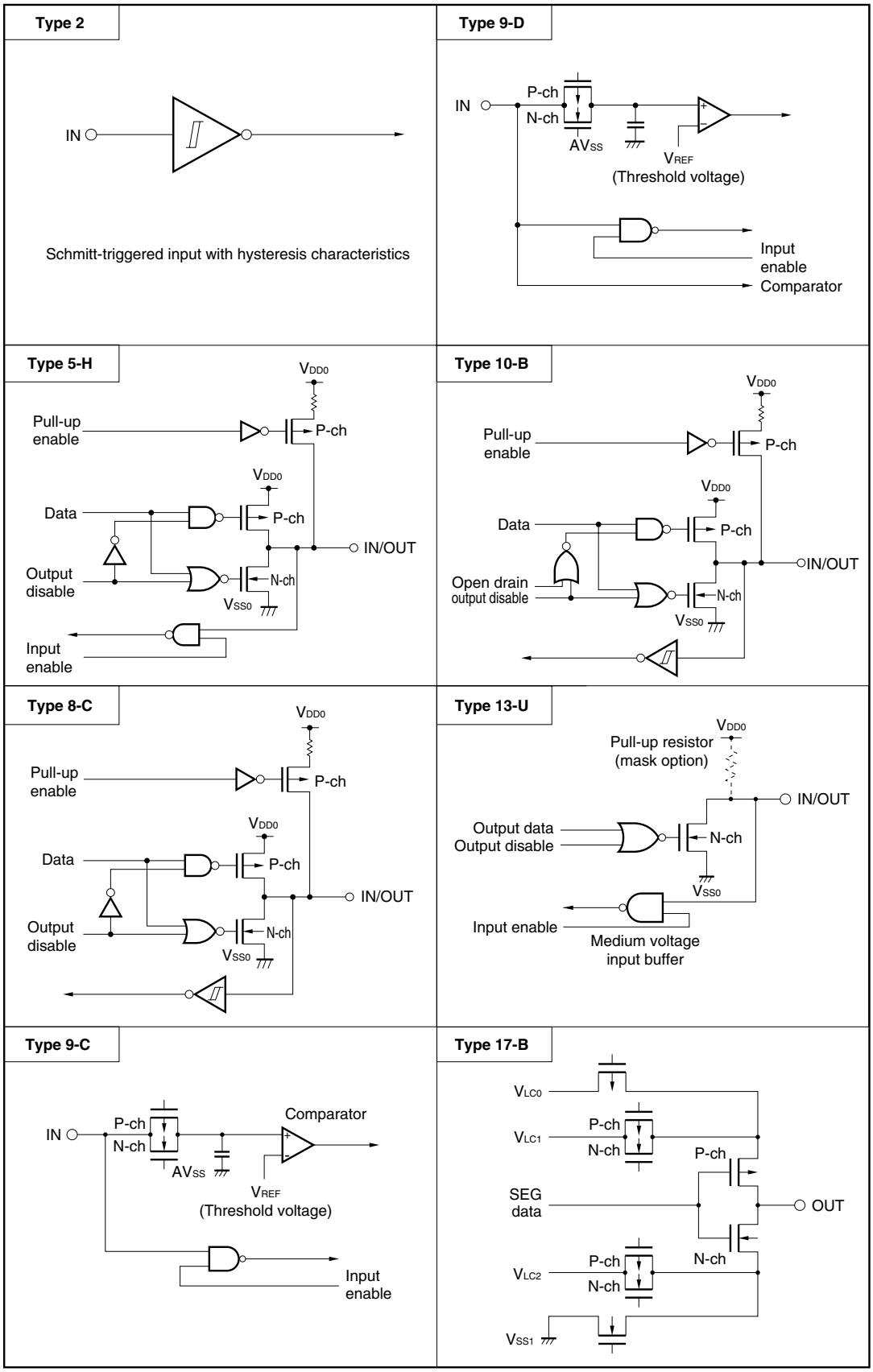
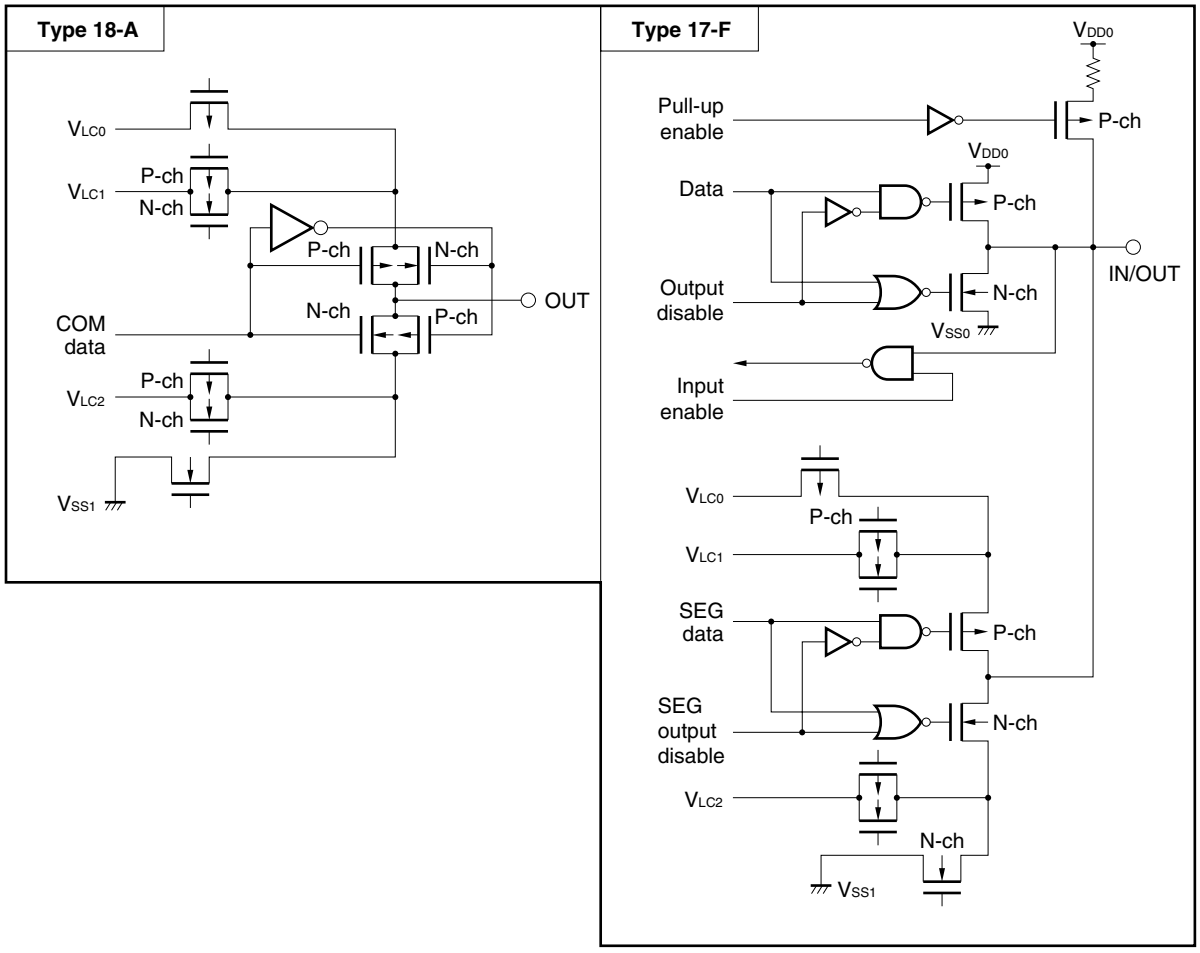


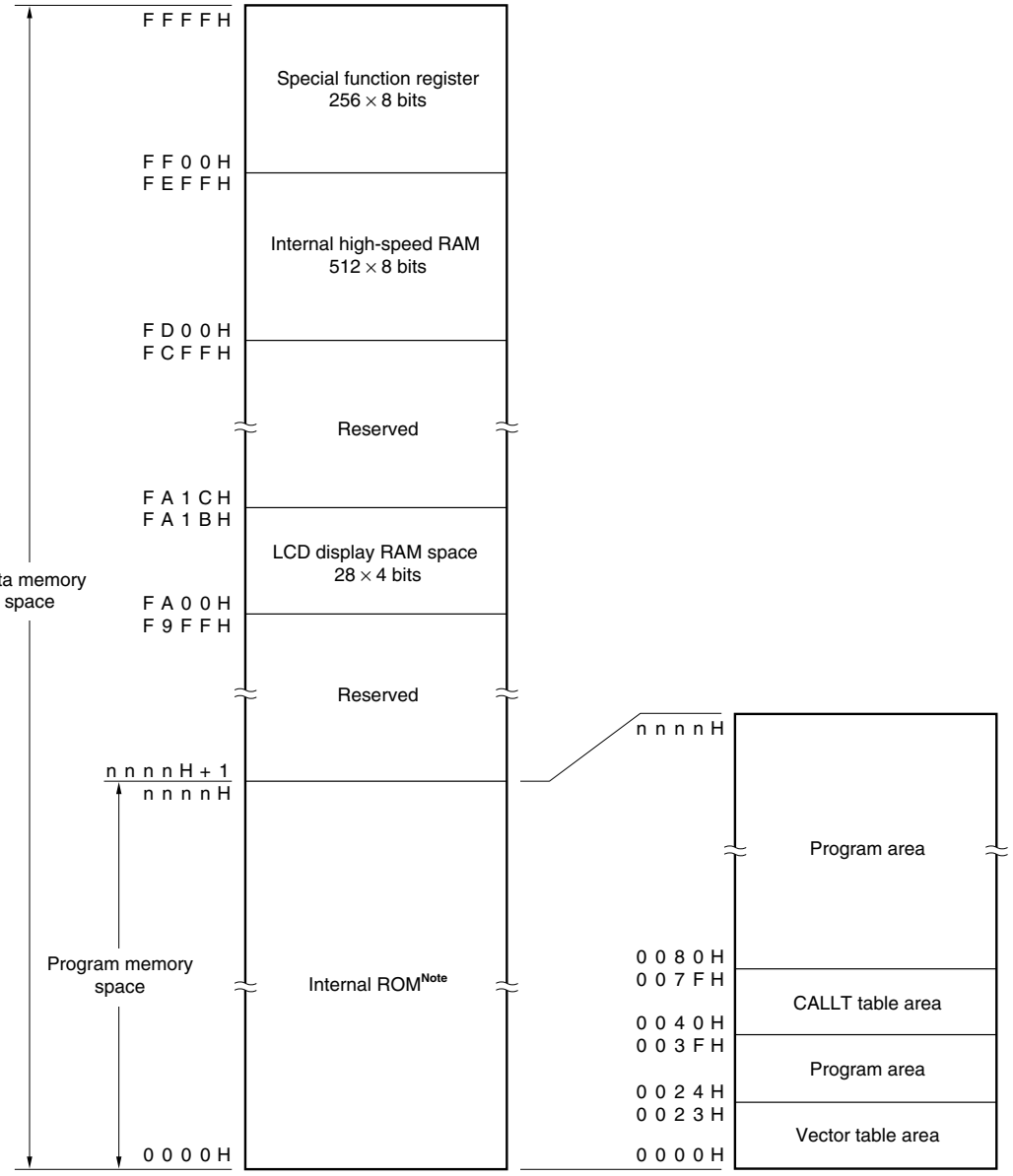
Figure 3-1. Pin I/O Circuits (2/2)



4. MEMORY SPACE

The μPD789405A, 789406A, 789407A, 789415A, 789416A, and 789417A can access 64 KB of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



Note The internal memory capacity differs depending on the product (see the table below).

Part Number	Last Address of Internal ROM nnnnH
μPD789405A, 789415A	2FFFH
μPD789406A, 789416A	3FFFH
μPD789407A, 789417A	5FFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The following I/O ports are available:

- CMOS I/O: 32
- CMOS input: 7
- N-ch open-drain I/O: 4

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P03	I/O port. Input output can be specified in 1-bit units. When used as input port, an on-chip pull-up resistor can be specified via software.
Port 2	P20 to P27	I/O port. Input/output can be specified in 1-bit units. When used as input port, an on-chip pull-up resistor can be specified via software.
Port 4	P40 to P47	I/O port. Input/output can be specified in 1-bit units. When used as input port, an on-chip pull-up resistor can be specified via software.
Port 5	P50 to P53	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by mask option.
Port 6	P60 to P66	Input-only port
Port 8	P80 to P87	I/O port. Input/output can be specified in 1-bit units. When used as input port, an on-chip pull-up resistor can be specified via software.
Port 9	P90 to P93	I/O port. Input/output can be specified in 1-bit units. When used as input port, an on-chip pull-up resistor can be specified via software.

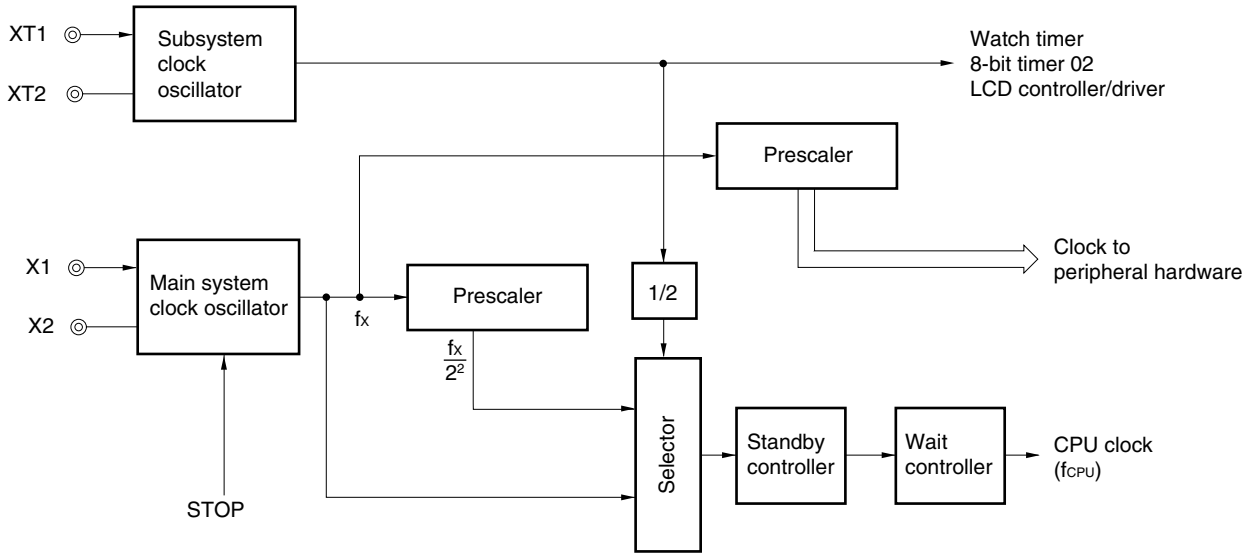
5.2 Clock Generator

An on-chip system clock generator is provided.

The minimum instruction execution time can be changed.

- 0.4 μs/1.6 μs (@ 5.0 MHz operation with main system clock)
- 122 μs (@ 32.768 kHz operation with subsystem clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer

Six on-chip timers are provided.

- 16-bit timer (TM50): 1 channel
- 8-bit timers/event counters (TM00 and TM01): 2 channels
- 8-bit timer (TM02): 1 channel
- Watch timer (WT): 1 channel
- Watchdog timer (WTM): 1 channel

★ **Table 5-2. Timer Operation**

		TM50	TM00	TM01	TM02	WT	WTM
Operation mode	Interval timer	–	1 channel	1 channel	1 channel	1 channel	1 channel
	External event counter	–	1 channel	1 channel	–	–	–
Function	Timer output	1 output	–	–	1 output	–	–
	Square wave output	–	–	–	1 output	–	–
	Capture input	1 input	–	–	–	–	–
	Interrupt request	1	1	1	1	1	1

Figure 5-2. Block Diagram of 16-Bit Timer 50

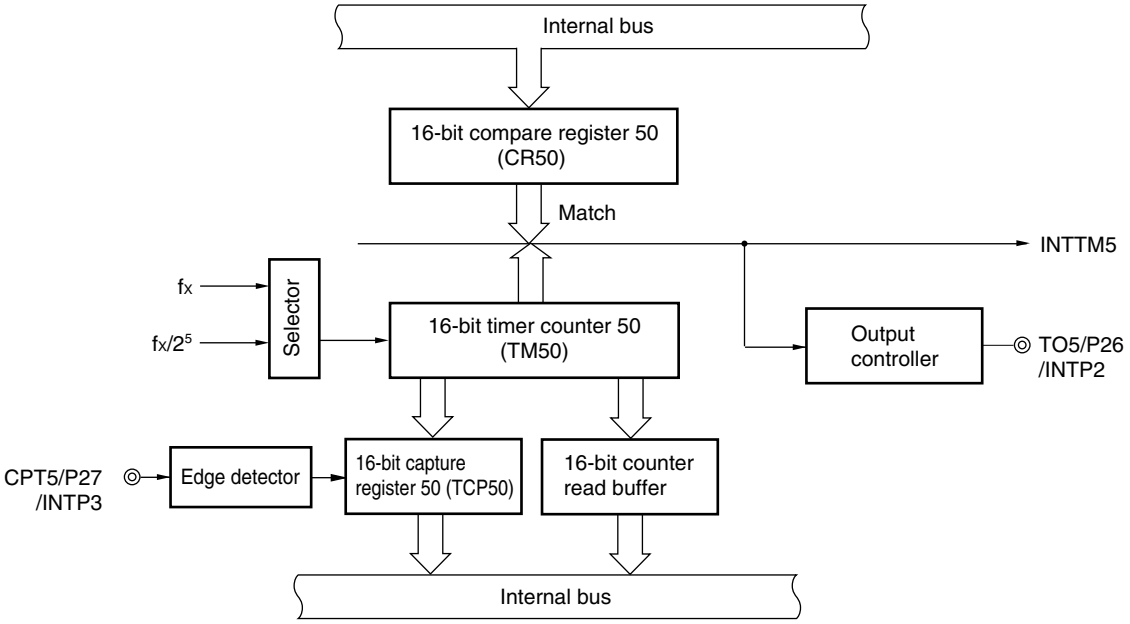


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 00

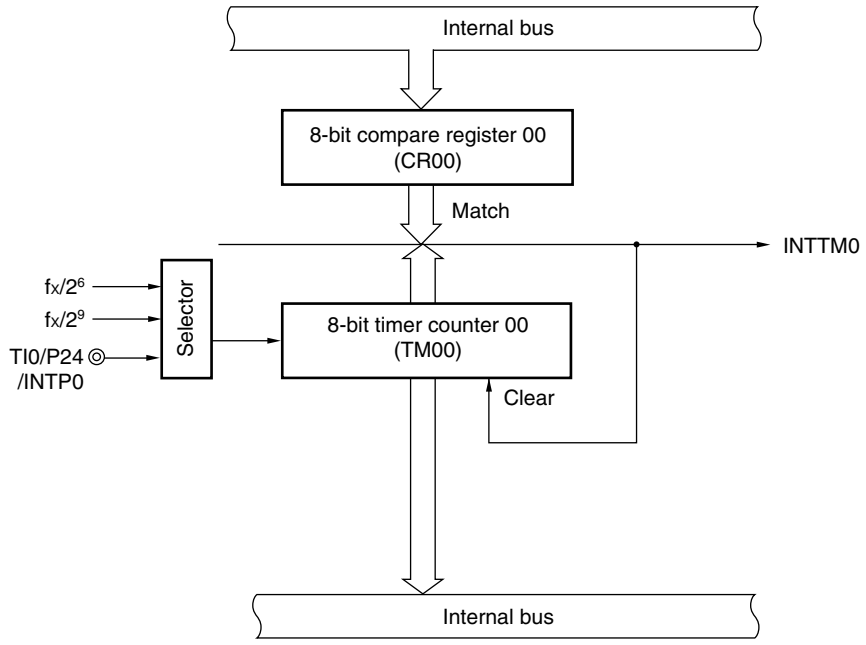


Figure 5-4. Block Diagram of 8-Bit Timer/Event Counter 01

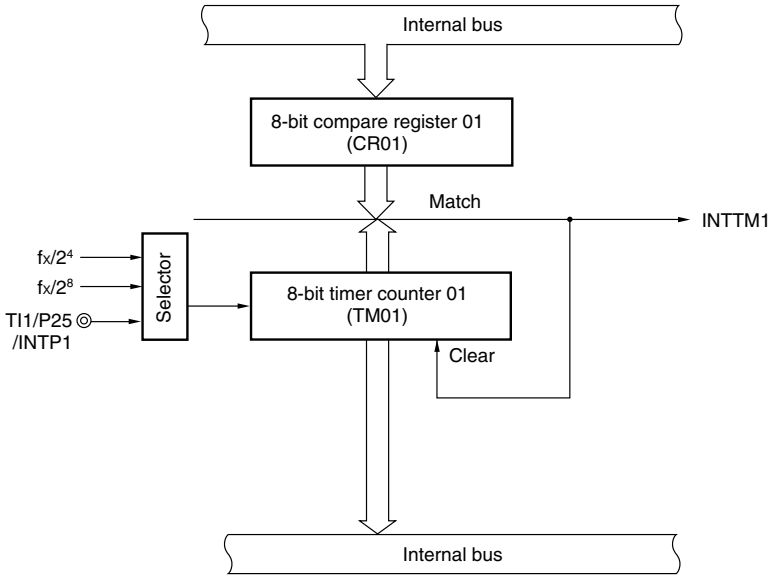


Figure 5-5. Block Diagram of 8-Bit Timer 02

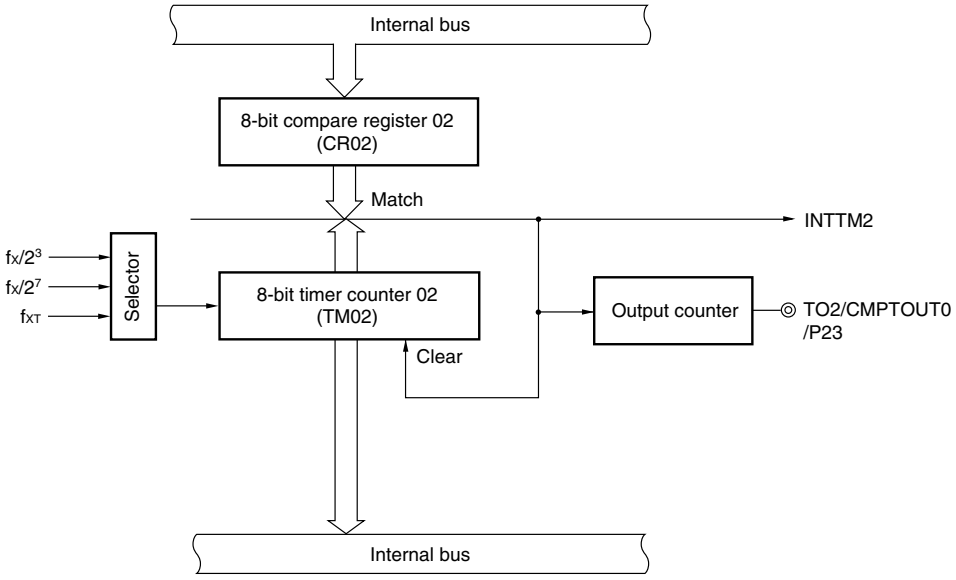


Figure 5-6. Block Diagram of Watch Timer

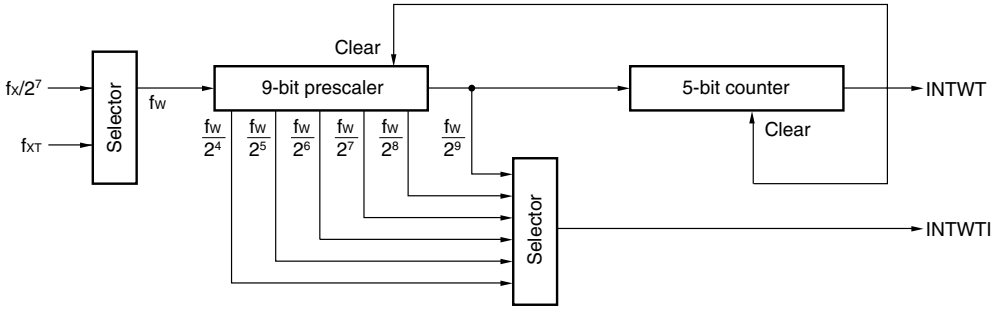
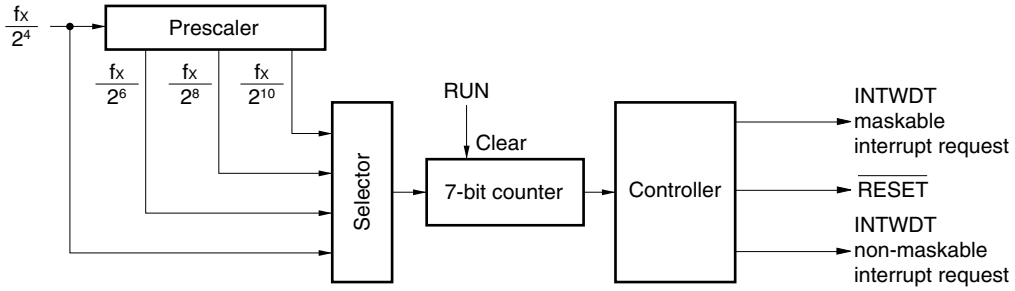


Figure 5-7. Block Diagram of Watchdog Timer



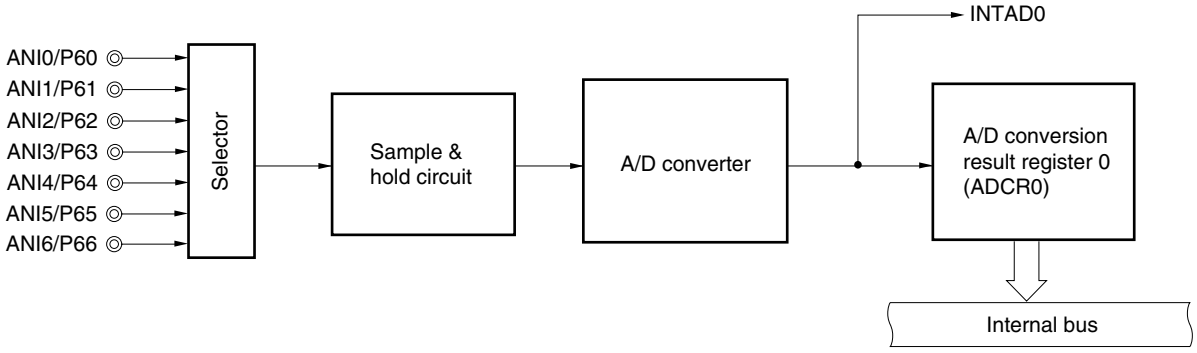
5.4 A/D Converter

The conversion resolution of the A/D converter differs depending on the product.

- 8-bit A/D converter ... μPD789405A, 789406A, 789407A
- 10-bit A/D converter ... μPD789415A, 789416A, 789417A

A/D conversion can only be started by software.

Figure 5-8. Block Diagram of A/D Converter

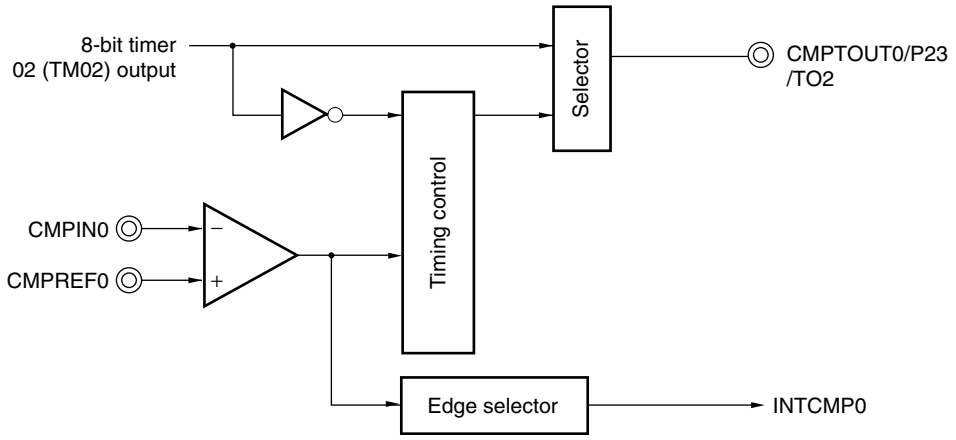


5.5 Comparator

A comparator with the following functions is provided.

- The input voltage of the reference voltage input pin (CMPREF0) is compared with the input voltage of the comparator input pin (CMPIN0). The result of the comparison can be read by using a memory manipulation instruction.
- The output of the comparator can be used to generate an interrupt request signal (INTCMP0).
- If CMPREF0 > CMPIN0, the output signal of 8-bit timer 02 (TM02) is output to the CMPTOUT0 pin.

Figure 5-9. Block Diagram of Comparator



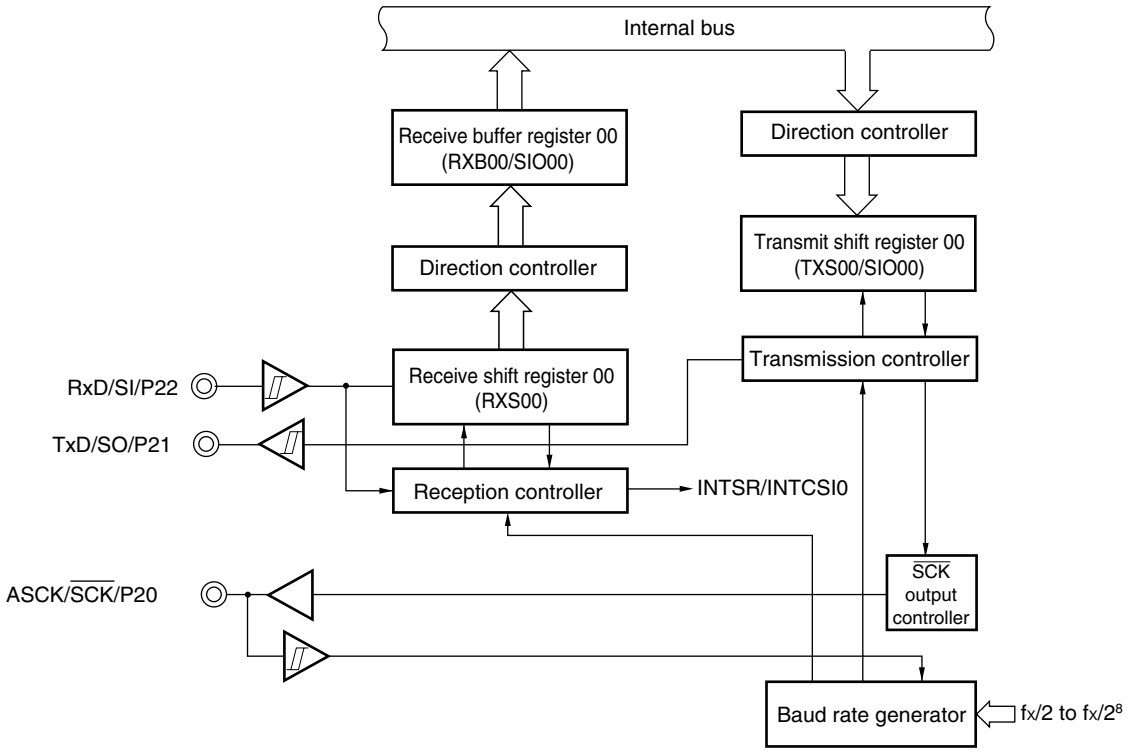
5.6 Serial Interface

One serial interface channel, serial interface 00, is provided.

Serial interface 00 has following two modes:

- 3-wire serial I/O mode: MSB/LSB first selectable
- Asynchronous serial interface (UART) mode: A dedicated baud generator is incorporated

Figure 5-10. Block Diagram of Serial Interface

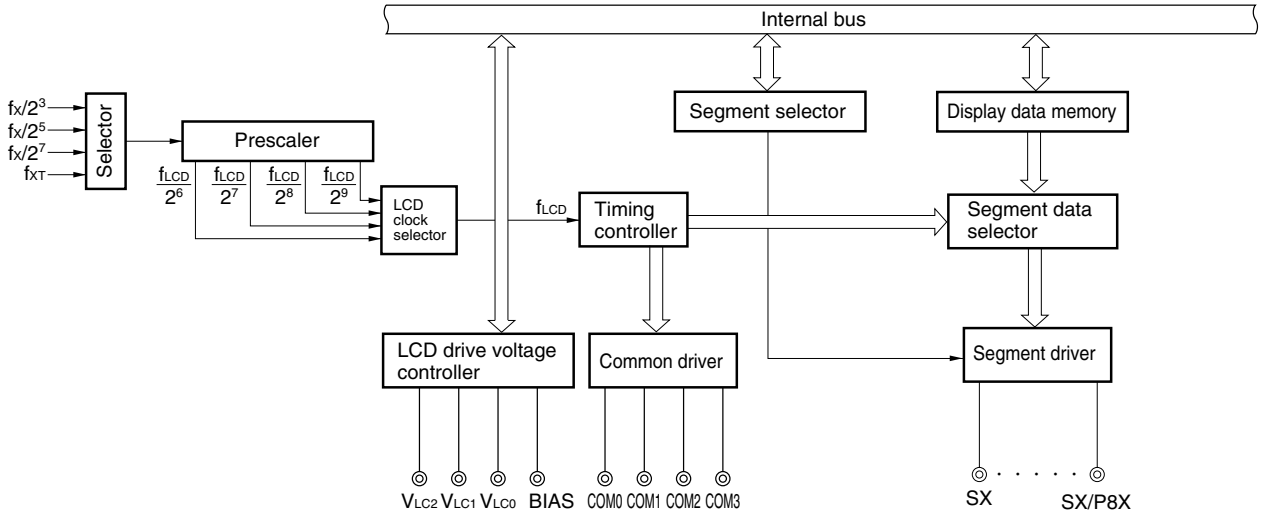


5.7 LCD Controller/Driver

An LCD controller/driver with the following functions is provided.

- Five display modes selectable
- Four frame frequencies selectable in each display mode
- Twelve segment signal output pins can be used as I/O port pins in 2-pin units (P80/S27 to P87/S20 and P90/S19 to P93/S16).
- A divider resistor for generating LCD drive voltage can be provided by mask option.

Figure 5-11. Block Diagram of LCD/Controller Driver



6. INTERRUPT FUNCTION

The following two types of interrupts and a total of 17 interrupt sources are available.

- Non-maskable: 1
- Maskable: 16

Table 6-1. Interrupt Sources

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (when interval timer mode is selected)			(B)
	1	INTP0	Detection of pin input edge	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSR00	UART reception completion for serial interface 00	Internal	000EH	(B)
		INTCSI00	3-wire SIO transfer/reception completion for serial interface 00			
	6	INTST00	UART transmission completion for serial interface 00		0010H	
	7	INTWT	Watch timer interrupt		0012H	
	8	INTWTI	Interval timer interrupt		0014H	
	9	INTTM00	Match signal generation of 8-bit timer/event counter 00		0016H	
	10	INTTM01	Match signal generation of 8-bit timer/event counter 01		0018H	
	11	INTTM02	Match signal generation of 8-bit timer 02		001AH	
	12	INTTM50	Match signal generation of 16-bit timer 50		001CH	
	13	INTKR00	Key return signal detection	External	001EH	(C)
	14	INTAD0	A/D conversion end signal	Internal	0020H	(B)
	15	INTCMP0	Comparator signal		0022H	

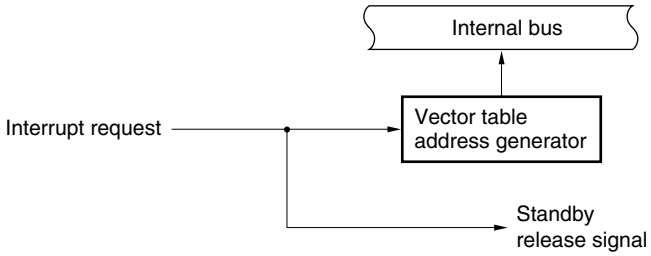
Notes 1. The priority is the priority order when more than one maskable interrupt occurs at the same time 0 is the highest priority and 15 is the lowest.

2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in **Figure 6-1**.

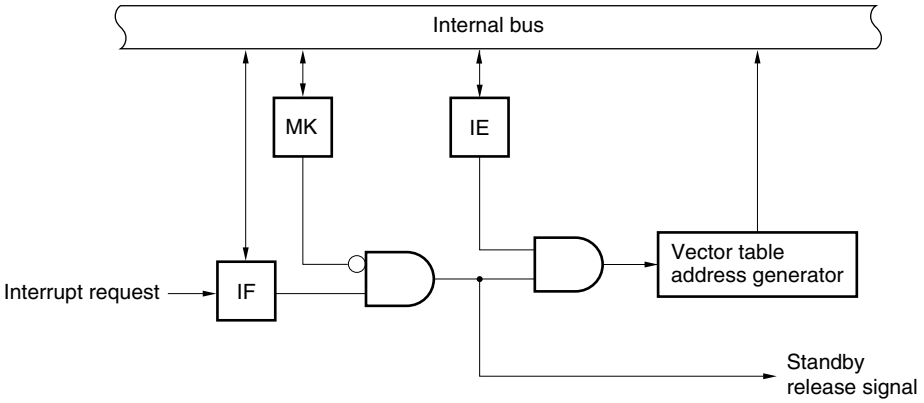
★ **Remark** Only one of the two watchdog timer interrupt (INTWDT) sources, non-maskable or maskable (internal) can be selected.

Figure 6-1. Basic Configuration of Interrupt Function

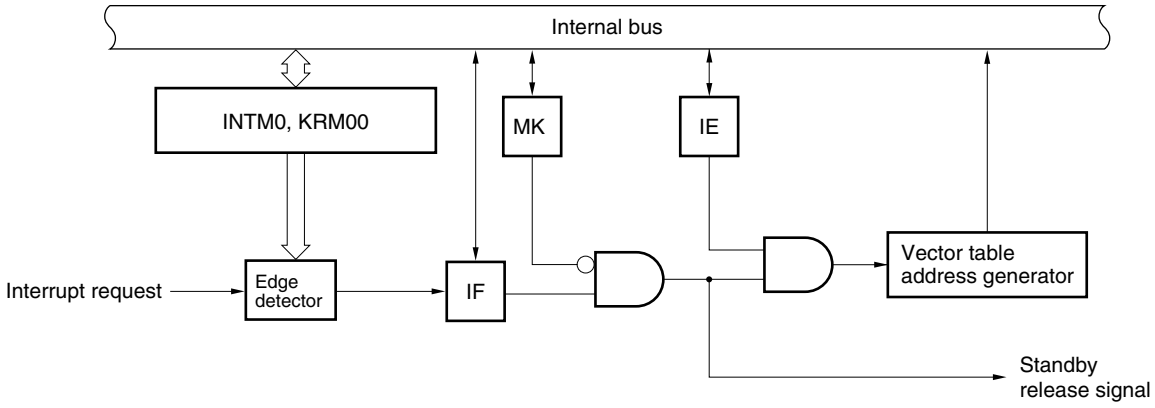
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



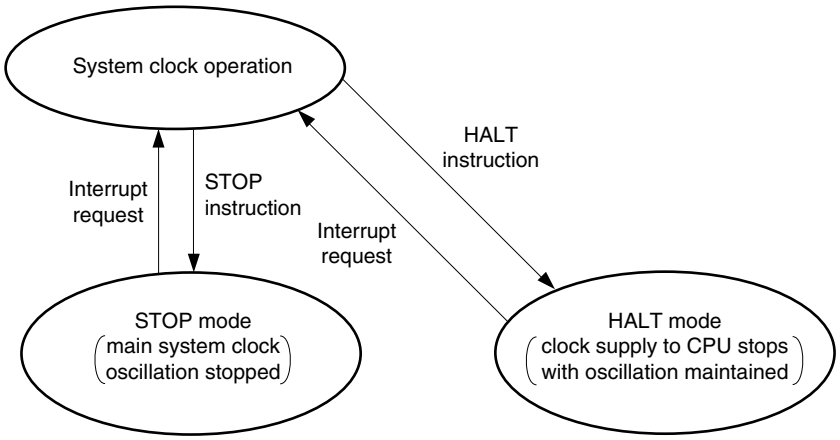
INTM0: External interrupt mode register 0
KRM00: Key return mode register 00
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

7. STANDBY FUNCTION

The standby function is used to lower the current consumption and can be used in the following two modes:

- HALT mode: In this mode, the CPU operating clock is stopped. The average current consumption can be reduced by intermittent operation combining this mode with the normal operating mode.
- STOP mode: In this mode, the main system clock oscillation is stopped. All operations performed with the main system clock are suspended thus minimizing power consumption.

Figure 7-1. Standby Function



8. RESET FUNCTION

The microcontroller can be reset in the following two ways.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer inadvertent program loop detection

9. MASK OPTION

The μPD789405A, 789406A, 789407A, 789415A, 789416A, and 789417A have the following mask options.

- Mask option of P50 to P53
  Connection of a pull-up resistor can be selected.

- Mask option of V_{LC0} to V_{LC2} pins and BIAS pin
  Connection of divider resistor for LCD drive can be selected.

For the resistance values of the pull-up resistor and divider resistor for LCD drive, refer to **11. ELECTRICAL SPECIFICATIONS**.

10. INSTRUCTION SET OVERVIEW

The instruction set for the μPD789405A, 789406A, 789407A, 789415A, 789416A, and 789417A is listed in this section.

10.1 Conventions

10.1.1 Operand identifiers and description methods

Operands are described in the “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, $, and [ ], are keywords and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, $, or [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 10-1. Operand Formats and Descriptions

Format	Description
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol
saddr	FE20H to FF1FH Immediate data or label
saddrp	FE20H to FF1FH Immediate data or label (even addresses only)
addr16	0000H to FFFFH Immediate data or label (even address only when 16-bit data transfer instruction is used)
addr5	0040H to 007FH Immediate data or label (even addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

10.1.2 Operation field definitions

A: A register (8-bit accumulator)
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair (16-bit accumulator)
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Flag to indicate that a non-maskable interrupt is being processed
( ): Contents of a memory location indicated by a parenthesized address or resister name
X_H, X_L: Higher and lower 8 bits of a 16-bit register
∧: Logical product (AND)
∨: Logical sum (OR)
∨: Exclusive OR
$\overline{\quad}$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

10.1.3 Flag operation field definitions

(Blank): Not affected
0: Clear to 0
1: Set to 1
×: Set or clear according to the result
R: Restore to the previous value

10.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag Z	Flag AC	Flag CY
MOV	r, #byte	3	6	r←byte			
	saddr, #byte	3	6	(saddr)←byte			
	sfr, #byte	3	6	sfr←byte			
	A, r Note 1	2	4	A←r			
	r, A Note 1	2	4	r←A			
	A, saddr	2	4	A←(saddr)			
	saddr, A	2	4	(saddr)←A			
	A, sfr	2	4	A←sfr			
	sfr, A	2	4	sfr←A			
	A, !addr16	3	8	A←(addr16)			
	!addr16, A	3	8	(addr16)←A			
	PSW, #byte	3	6	PSW←byte	×	×	×
	A, PSW	2	4	A←PSW			
	PSW, A	2	4	PSW←A	×	×	×
	A, [DE]	1	6	A←(DE)			
	[DE], A	1	6	(DE)←A			
	A, [HL]	1	6	A←(HL)			
	[HL], A	1	6	(HL)←A			
	A, [HL+byte]	2	6	A←(HL+byte)			
	[HL+byte], A	2	6	(HL+byte)←A			
XCH	A, X	1	4	A↔X			
	A, r Note 2	2	6	A↔r			
	A, saddr	2	6	A↔(saddr)			
	A, sfr	2	6	A↔(sfr)			
	A, [DE]	1	8	A↔(DE)			
	A, [HL]	1	8	A↔(HL)			
	A, [HL+byte]	2	8	A↔(HL+byte)			
MOVW	rp, #word	3	6	rp←word			
	AX, saddrp	2	6	AX←(saddrp)			
	saddrp, AX	2	8	(saddrp)←AX			
	AX, rp Note 3	1	4	AX←rp			
	rp, AX Note 3	1	4	rp←AX			
XCHW	AX, rp Note 3	1	8	AX↔rp			

Notes 1. Except when r = A

2. Except when r = A or X

3. Only when rp = BC, DE, or HL

Remark One instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY←A+byte	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)+byte	×	×	×
	A, r	2	4	A, CY←A+r	×	×	×
	A, saddr	2	4	A, CY←A+(saddr)	×	×	×
	A, !addr16	3	8	A, CY←A+(addr16)	×	×	×
	A, [HL]	1	6	A, CY←A+(HL)	×	×	×
	A, [HL+byte]	2	6	A, CY←A+(HL+byte)	×	×	×
ADDC	A, #byte	2	4	A, CY←A+byte+CY	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)+byte+CY	×	×	×
	A, r	2	4	A, CY←A+r+CY	×	×	×
	A, saddr	2	4	A, CY←A+(saddr)+CY	×	×	×
	A, !addr16	3	8	A, CY←A+(addr16)+CY	×	×	×
	A, [HL]	1	6	A, CY←A+(HL)+CY	×	×	×
	A, [HL+byte]	2	6	A, CY←A+(HL+byte)+CY	×	×	×
SUB	A, #byte	2	4	A, CY←A–byte	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)–byte	×	×	×
	A, r	2	4	A, C←A–r	×	×	×
	A, saddr	2	4	A, CY←A–(saddr)	×	×	×
	A, !addr16	3	8	A, CY← A–(addr16)	×	×	×
	A, [HL]	1	6	A, CY←A–(HL)	×	×	×
	A, [HL+byte]	2	6	A, CY←A–(HL+byte)	×	×	×
SUBC	A, #byte	2	4	A, CY←A–byte–CY	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)–byte–CY	×	×	×
	A, r	2	4	A, CY←A–r–CY	×	×	×
	A, saddr	2	4	A, CY←A–(saddr)–CY	×	×	×
	A, !addr16	3	8	A, CY←A–(addr16)–CY	×	×	×
	A, [HL]	1	6	A, CY←A–(HL)–CY	×	×	×
	A, [HL+byte]	2	6	A, CY←A–(HL+byte)–CY	×	×	×
AND	A, #byte	2	4	A←A∧byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)∧byte	×		
	A, r	2	4	A←A∧r	×		
	A, saddr	2	4	A←A∧(saddr)	×		
	A, !addr16	3	8	A←A∧(addr16)	×		
	A, [HL]	1	6	A←A∧(HL)	×		
	A, [HL+byte]	2	6	A←A∧(HL+byte)	×		

Remark One instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A←A∨byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)∨byte	×		
	A, r	2	4	A←A∨r	×		
	A, saddr	2	4	A←A∨ (saddr)	×		
	A, !addr16	3	8	A←A∨(addr16)	×		
	A, [HL]	1	6	A←A∨(HL)	×		
	A, [HL+byte]	2	6	A←A∨(HL+byte)	×		
XOR	A, #byte	2	4	A←A⊻byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)⊻byte	×		
	A, r	2	4	A←A⊻r	×		
	A, saddr	2	4	A←A⊻(saddr)	×		
	A, !addr16	3	8	A←A⊻(addr16)	×		
	A, [HL]	1	6	A←A⊻(HL)	×		
	A, [HL+byte]	2	6	A←A⊻(HL+byte)	×		
CMP	A, #byte	2	4	A–byte	×	×	×
	saddr, #byte	3	6	(saddr)–byte	×	×	×
	A, r	2	4	A–r	×	×	×
	A, saddr	2	4	A–(saddr)	×	×	×
	A, !addr16	3	8	A–(addr16)	×	×	×
	A, [HL]	1	6	A–(HL)	×	×	×
	A, [HL+byte]	2	6	A–(HL+byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY←AX+word	×	×	×
SUBW	AX, #word	3	6	AX, CY←AX–word	×	×	×
CMPW	AX, #word	3	6	AX–word	×	×	×
INC	r	2	4	r←r+1	×	×	
	saddr	2	4	(saddr)←(saddr)+1	×	×	
DEC	r	2	4	r←r–1	×	×	
	saddr	2	4	(saddr)←(saddr)–1	×	×	
INCW	rp	1	4	rp←rp+1			
DECW	rp	1	4	rp←rp–1			
ROR	A, 1	1	2	(CY, A_7←A_0, A_{m-1}←A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0←A_7, A_{m+1}←A_m) × 1			×
RORC	A, 1	1	2	(CY←A_0, A_7←CY , A_{m-1}←A_m) × 1			×
ROLC	A, 1	1	2	(CY←A_7, A_0←CY , A_{m+1}←A_m) × 1			×

Remark One instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit)←1			
	sfr. bit	3	6	sfr. bit←1			
	A. bit	2	4	A. bit←1			
	PSW. bit	3	6	PSW. bit←1	×	×	×
	[HL]. bit	2	10	(HL). bit←1			
CLR1	saddr. bit	3	6	(saddr. bit)←0			
	sfr. bit	3	6	sfr. bit←0			
	A. bit	2	4	A. bit←0			
	PSW. bit	3	6	PSW. bit←0	×	×	×
	[HL]. bit	2	10	(HL). bit←0			
SET1	CY	1	2	CY←1			1
CLR1	CY	1	2	CY←0			0
NOT1	CY	1	2	CY←$\overline{CY}$			×
CALL	!addr16	3	6	$(SP-1)\leftarrow(PC+3)_H$, $(SP-2)\leftarrow(PC+3)_L$, PC←addr16, SP←SP−2			
CALLT	[addr5]	1	8	$(SP-1)\leftarrow(PC+1)_H$, $(SP-2)\leftarrow(PC+1)_L$, $PC_H\leftarrow$(00000000, addr5+1), $PC_L\leftarrow$(00000000, addr5), SP←SP−2			
RET		1	6	$PC_H\leftarrow(SP+1)$, $PC_L\leftarrow(SP)$, SP←SP+2			
RETI		1	8	$PC_H\leftarrow(SP+1)$, $PC_L\leftarrow(SP)$, PSW←(SP+2), SP←SP+3, NMIS←0	R	R	R
PUSH	PSW	1	2	(SP−1)←PSW, SP←SP−1			
	rp	1	4	$(SP-1)\leftarrow rp_H$, $(SP-2)\leftarrow rp_L$, SP←SP−2			
POP	PSW	1	4	PSW←(SP), SP←SP+1	R	R	R
	rp	1	6	$rp_H\leftarrow(SP+1)$, $rp_L\leftarrow$ (SP), SP←SP+2			
MOVW	SP, AX	2	8	SP←AX			
	AX, SP	2	6	AX←SP			
BR	!addr16	3	6	PC←addr16			
	$addr16	2	6	PC←PC+2+jdisp8			
	AX	1	6	$PC_H\leftarrow$A, $PC_L\leftarrow$X			

Remark One instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag
					Z AC CY
BC	$addr16	2	6	PC←PC+2+jdisp8 if CY = 1	
BNC	$addr16	2	6	PC←PC+2+jdisp8 if CY = 0	
BZ	$addr16	2	6	PC←PC+2+jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC←PC+2+jdisp8 if Z = 0	
BT	saddr. bit, $addr16	4	10	PC←PC+4+jdisp8 if (saddr. bit) = 1	
	sfr. bit, $addr16	4	10	PC←PC+4+jdisp8 if sfr. bit = 1	
	A. bit, $addr16	3	8	PC←PC+3+jdisp8 if A. bit = 1	
	PSW. bit, $addr16	4	10	PC←PC+4+jdisp8 if PSW. bit = 1	
BF	saddr. bit, $addr16	4	10	PC←PC+4+jdisp8 if (saddr. bit) = 0	
	sfr. bit, $addr16	4	10	PC←PC+4+jdisp8 if sfr. bit = 0	
	A. bit, $addr16	3	8	PC←PC+3+jdisp8 if A. bit = 0	
	PSW. bit, $addr16	4	10	PC←PC+4+jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B←B−1, then PC←PC+2+jdisp8 if B≠0	
	C, $addr16	2	6	C←C−1, then PC←PC+2+jdisp8 if C≠0	
	saddr, $addr16	3	8	(saddr)←(saddr)−1, then PC←PC+3+jdisp8 if (saddr)≠0	
NOP		1	2	No Operation	
EI		3	6	IE←1 (Enable Interrupt)	
DI		3	6	IE←0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark One instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

11. ELECTRICAL SPECIFICATIONS

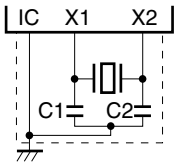
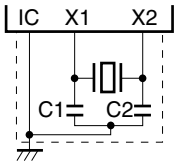
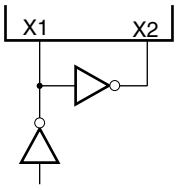
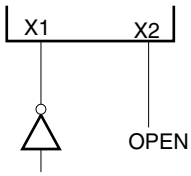
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition		Ratings	Unit
Supply voltage	V_{DD}	$AV_{DD} - 0.3\ V \le V_{DD} \le AV_{DD} + 0.3\ V$		−0.3 to +6.5	V
	AV_{DD}	$AV_{REF} \le V_{DD} + 0.3\ V$			
	AV_{REF}	$AV_{REF} \le AV_{DD} + 0.3\ V$			
Input voltage	V_{I1}	Pins other than P50 to P53		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	N-ch open drain	−0.3 to +13	V
			On-chip pull-up resistor	−0.3 to V_{DD} + 0.3	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		−10	mA
		Total of all pins		−30	mA
Output current, low	I_{OL}	Per pin		30	mA
		Total of all pins		160	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Condition	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} has reached MIN. of oscillation start voltage			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)Note 1	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the specified oscillation wait time.

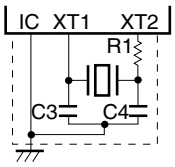
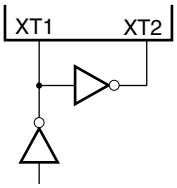
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the writing near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

★ **Remark** For the resonator selection and oscillator constant, users are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem clock oscillator characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Condition	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	s
External clock		XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the specified oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

★ **Remark** For the resonator selection and oscillator constant, users are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–15	mA
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V_{IH1}	P00 to P03, P46, P47, P60 to P66, P80 to P87, P90 to P93	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	N-ch open drain, V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
				0.9V_{DD}		12	V
			On-chip pull-up resistor, V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{RESET}$, P20 to P27, P40 to P45	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P03, P46, P47, P60 to P66, P80 to P87, P90 to P93	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL3}	$\overline{RESET}$, P20 to P27, P40 to 45	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL4}	X1, X2, XT1, XT2		0		0.1	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA	V_{DD} = 4.5 to 5.5 V	V_{DD} – 1.0			V
		I_{OH} = –100 μA	V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
★ Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 12 V	P50 to P53 (N-ch open drain)			20	μA
★ Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–3[Note]	μA

Note A low-level input leakage current of –30 μA (MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 when on-chip pull-up resistors are not connected to P50 to P53 (specified by mask option) and P50 to P53 are set to input mode. At times other than this, a –3 μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R_1	V_{IN} = 0 V, pins other than P50 to P53		50	100	200	kΩ
Mask option pull-up resistor	R_2	V_{IN} = 0 V, P50 to P53		15	30	60	kΩ
Supply current	I_{DD1} Note 1	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		2.0	4.0	mA
			V_{DD} = 3.0 V ±10% Note 5		0.6	1.2	mA
			V_{DD} = 2.0 V ±10% Note 5		0.3	0.6	mA
	I_{DD2} Note 1	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		1.1	2.2	mA
			V_{DD} = 3.0 V ±10% Note 5		0.4	0.8	mA
			V_{DD} = 2.0 V ±10% Note 5		0.2	0.4	mA
	I_{DD3} Note 1	32.768 kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22 pF, R1 = 220 kΩ)	V_{DD} = 5.0 V ±10%		30	90	μA
			V_{DD} = 3.0 V ±10%		9	50	μA
			V_{DD} = 2.0 V ±10%		4	25	μA
	I_{DD4} Note 1	32.768 kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22 pF, R1 = 220 kΩ)	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		5	25	μA
			V_{DD} = 2.0 V ±10%		2.5	12.5	μA
	I_{DD5} Note 1	32.768 kHz crystal oscillation STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5.0	μA
			V_{DD} = 3.0 V ±10%, T_A = 25 °C		0.05	3.0	μA
			V_{DD} = 2.0 V ±10%		0.05	3.0	μA
	I_{DD6} Notes 1, 2	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%		2.6	6.0	mA
			V_{DD} = 3.0 V ±10%		1.2	3.6	mA
			V_{DD} = 2.0 V ±10%		0.9	2.7	mA

Notes 1. Excluding AV_{REF}, A/D operation ON (ADCS0 (bit 7 of A/D converter mode register 0 (ADM0) = 1) current, AV_{DD} current, and port current (including current flowing through the internal pull-up resistors).

2. For the current flowing into AV_{REF}, refer to **8-Bit A/D Converter Characteristics** and **10-Bit A/D Converter Characteristics**.

3. When the main system clock is stopped

4. During high-speed mode operation (when processor clock control register (PCC) is set to 00H)

5. During low-speed mode operation (when PCC = 02H)

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pin.

LCD Characteristics (T_A = –40 to +85°C, V_{DD} = 2.2 to 5.5 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
★ LCD drive voltage	V_{LCD}	VAON0 = 1		2.2		V_{DD}	V
		VAON0 = 0 Note 1	At 1/3 bias	2.7		V_{DD}	V
			At 1/2 bias	3.0		V_{DD}	V
LCD divider resistor Note 2	R_{LCD1}			100	200	400	kΩ
	R_{LCD2}			10	20	40	kΩ
LCD output voltage deviation Note 3 (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 2/3$	0		±0.2	V
LCD output voltage deviation Note 3 (segment)	V_{ODS}	I_O = ±1 μA	$2.2\ V \le V_{LCD} \le V_{DD}$ $V_{LCD2} = V_{LCD} \times 1/3$ Note 1	0		±0.2	V

★ **Notes 1.** T_A = –10 to +85°C in the normal mode (VAON0 = 0)

2. R_{LCD1}, R_{LCD2}, or no divider resistor can be selected by mask option.

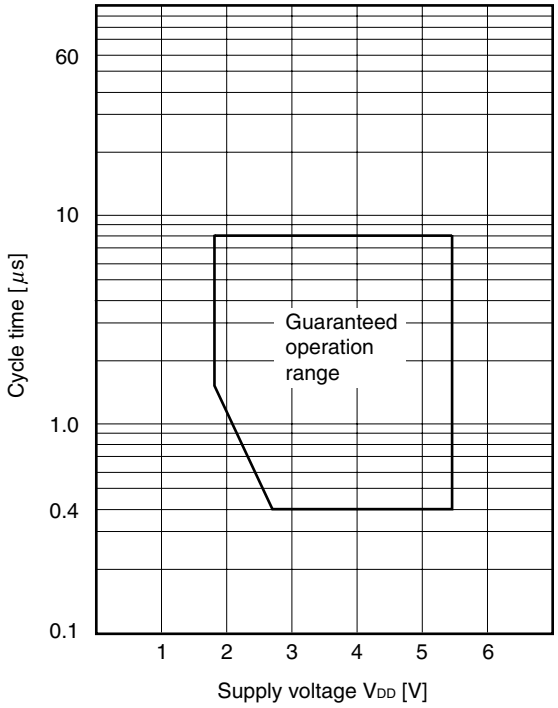
3. Voltage deviation is the voltage difference between the ideal value of the segment or common output (V_{LCDn}: n = 0 to 2) and the output voltage.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating with main system clock	V_{DD} = 2.7 to 5.5 V	0.4		8	μs
				1.6		8	μs
		Operating with subsystem clock		114	122	125	μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
TI0, TI1 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
				1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3		10			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}			10			μs

T_{CY} vs V_{DD} (Main system clock)



★ **(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)**

(a) 3-wire serial I/O mode ($\overline{SCK}$ ... Internal clock output)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 - 50$			ns
				$t_{KCY1}/2 - 150$			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	R = 1 kΩ C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(b) 3-wire serial I/O mode ($\overline{SCK}$ ... external clock input)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		900			ns
				3500			ns
$\overline{SCK}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	R = 1 kΩ C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

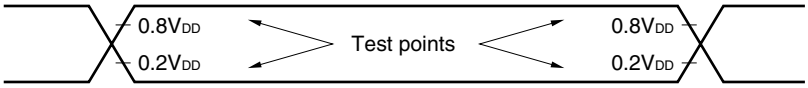
(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
					19531	bps

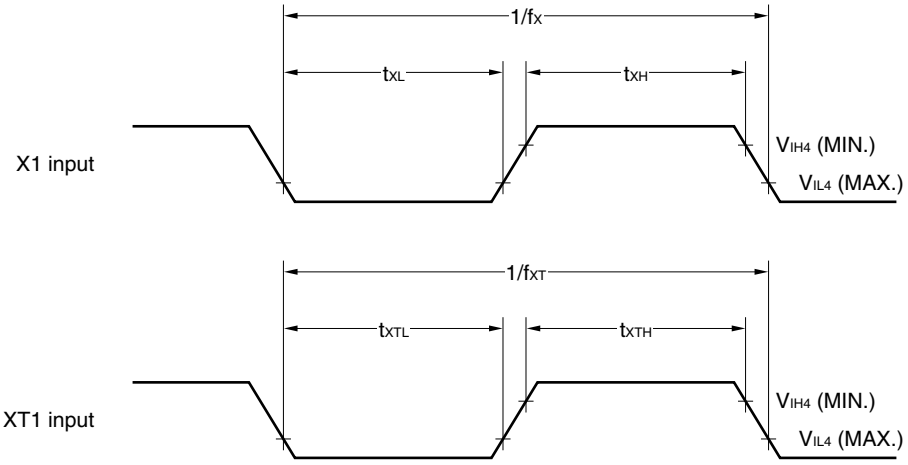
(d) UART mode (external clock input)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
			3500			ns
ASCK high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
			1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
					9766	bps
ASCK rise/fall time	t_R, t_F				1	μs

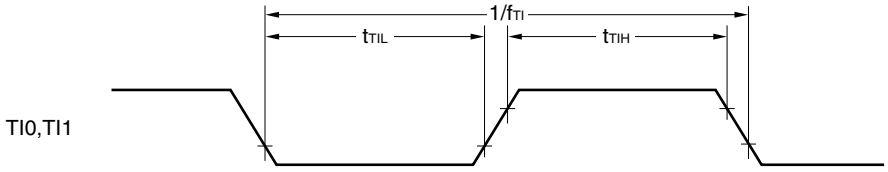
AC Timing Test Points (Excluding X1 and XT1 Inputs)



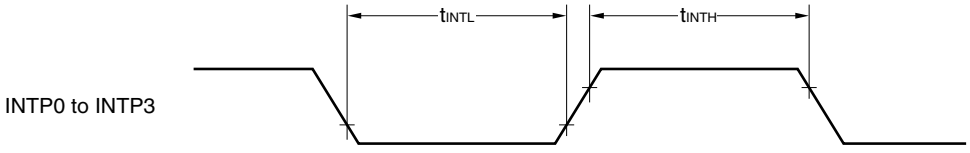
Clock Timing



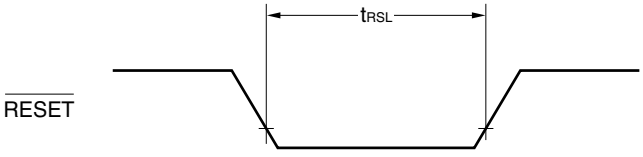
★ **TI Timing**



Interrupt Input Timing

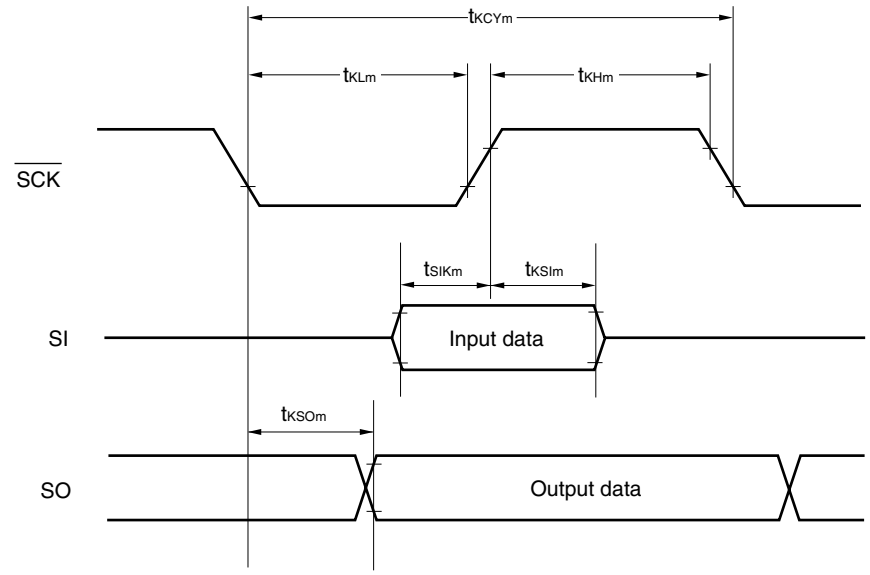


$\overline{\text{RESET}}$ Input Timing



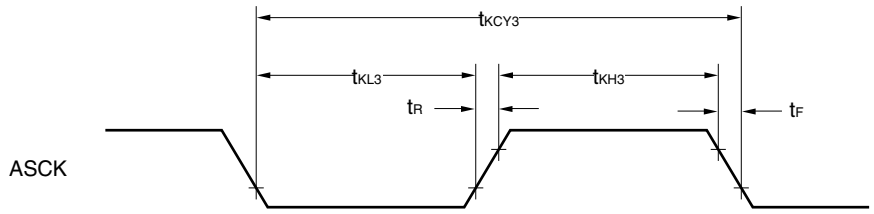
Serial Transfer Timing

3-wire serial I/O mode:



Remark m = 1, 2

UART mode (external clock input):



8-Bit A/D Converter Characteristics (μPD789405A, 789406A, 789407A)
(T_A = –40 to +85°C, 1.8 V ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
				±0.8	±1.2	%FSR
Conversion time	t_{CONV}	2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
			28		100	μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.2% FSR).

Remark FSR: Full-scale range

10-Bit A/D Converter Characteristics (μPD789415A, 789416A, 789417A)
(T_A = –40 to +85 °C, 1.8 V ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	28		100	μs
Zero-scale error[Note]	AINL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Full-scale error[Note]	AINL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Non-integral linearity[Note]	INL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±4.5	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±8.5	LSB
Non-differential linearity[Note]	DNL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full-scale range.

Comparator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Analog input range	V_{CIN}		0		V_{DD}	V
Reference voltage input range	V_{CREF}	V_{DD} = 2.7 to 5.5 V	1.35	1.6	1.85	V
			1.35	1.4	1.45	V
Accuracy					±100	mV

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

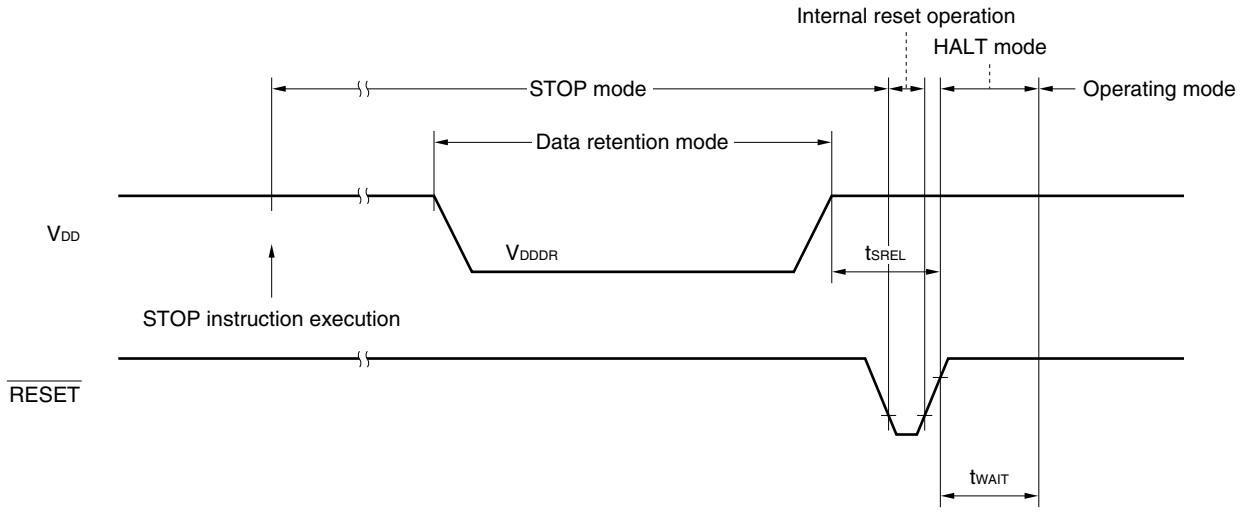
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Release by interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization wait time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.

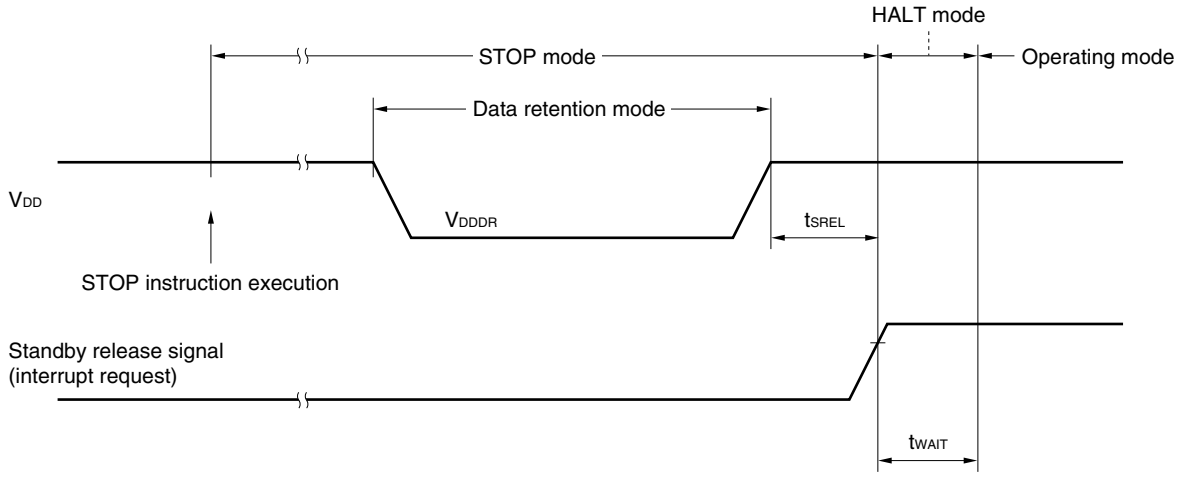
2. $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected by using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark fx: Main system clock oscillation frequency

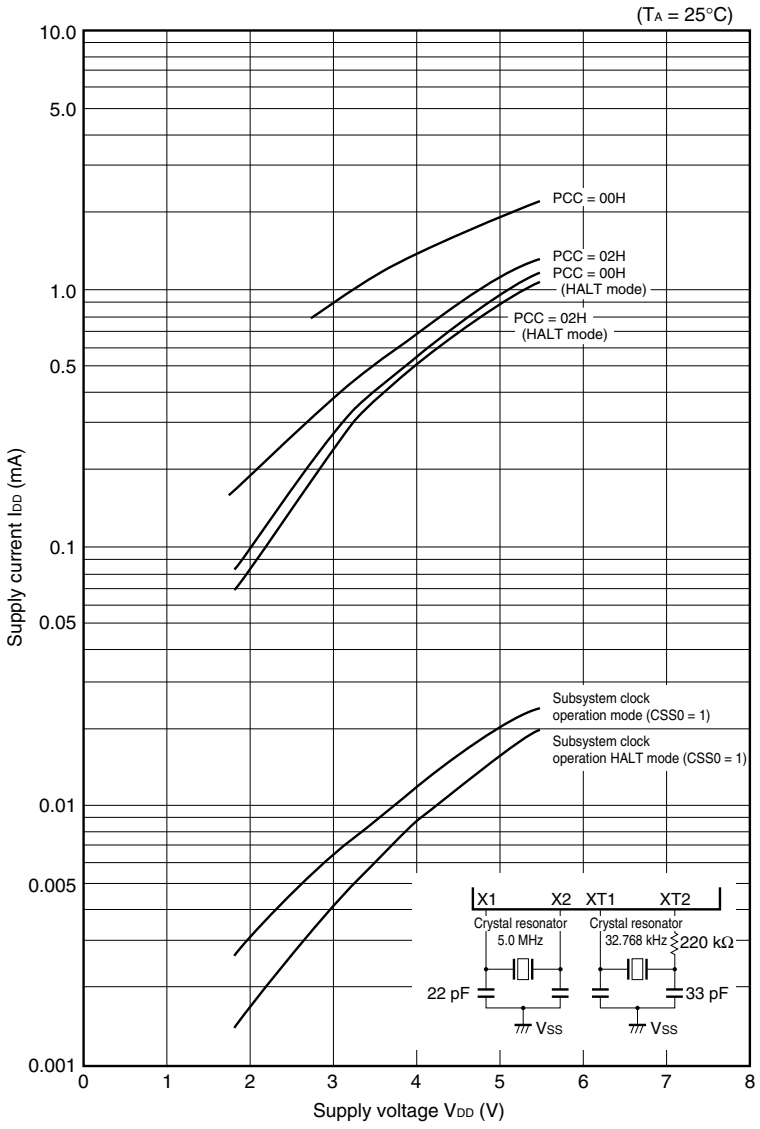
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



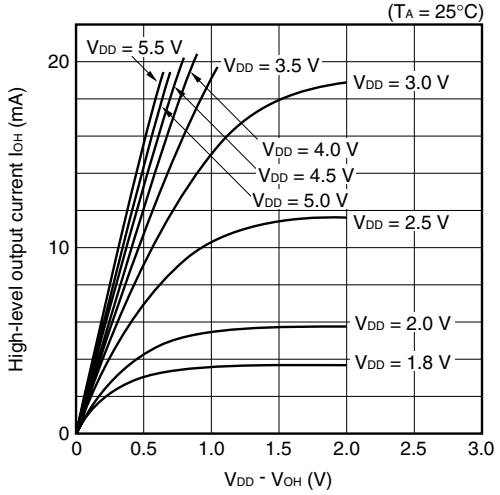
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



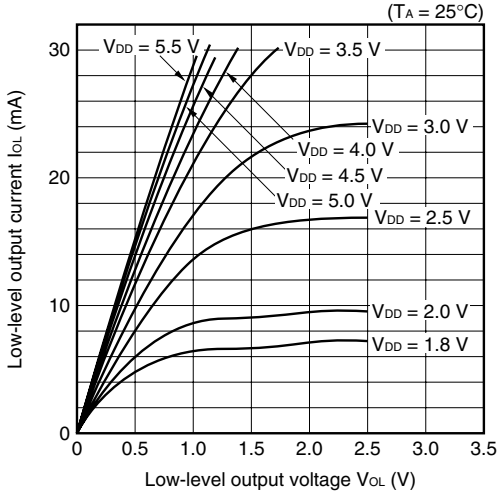
12. CHARACTERISTICS CURVES



IOH vs VDD - VOH

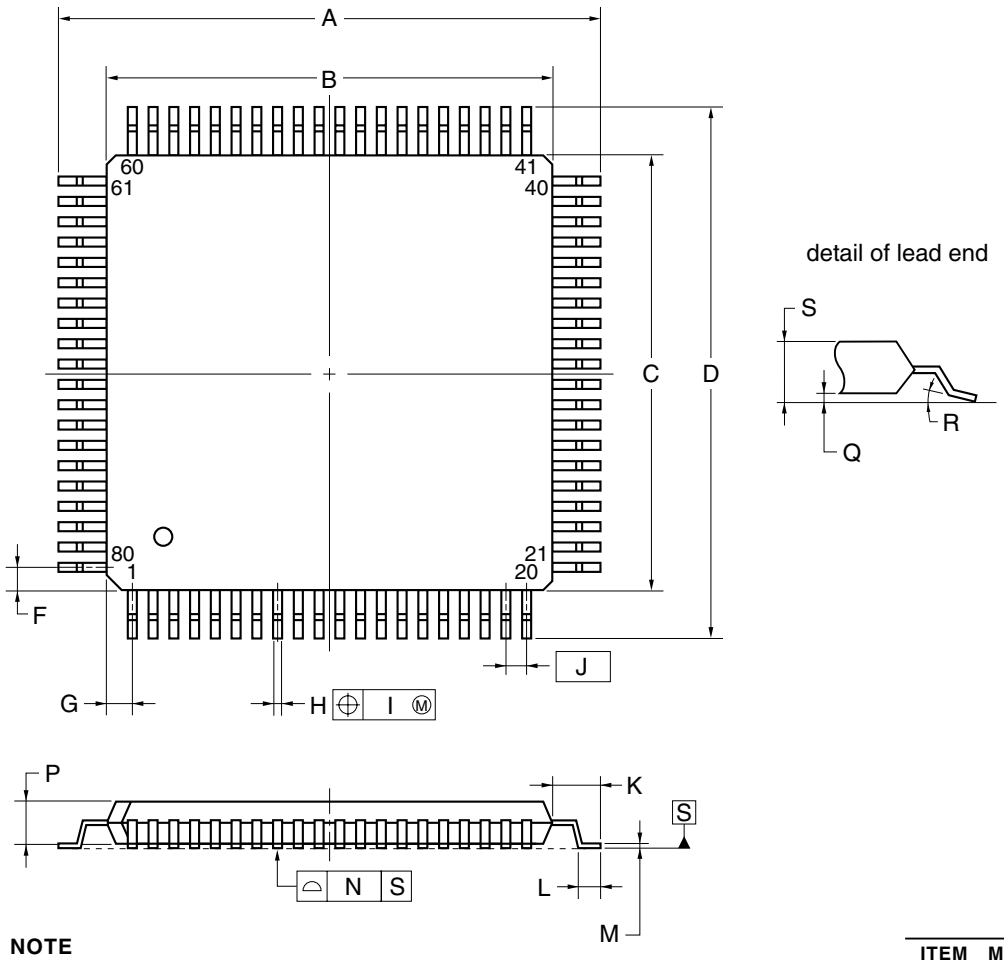


IOL vs VOL



13. PACKAGE DRAWINGS

★ 80-PIN PLASTIC QFP (14x14)



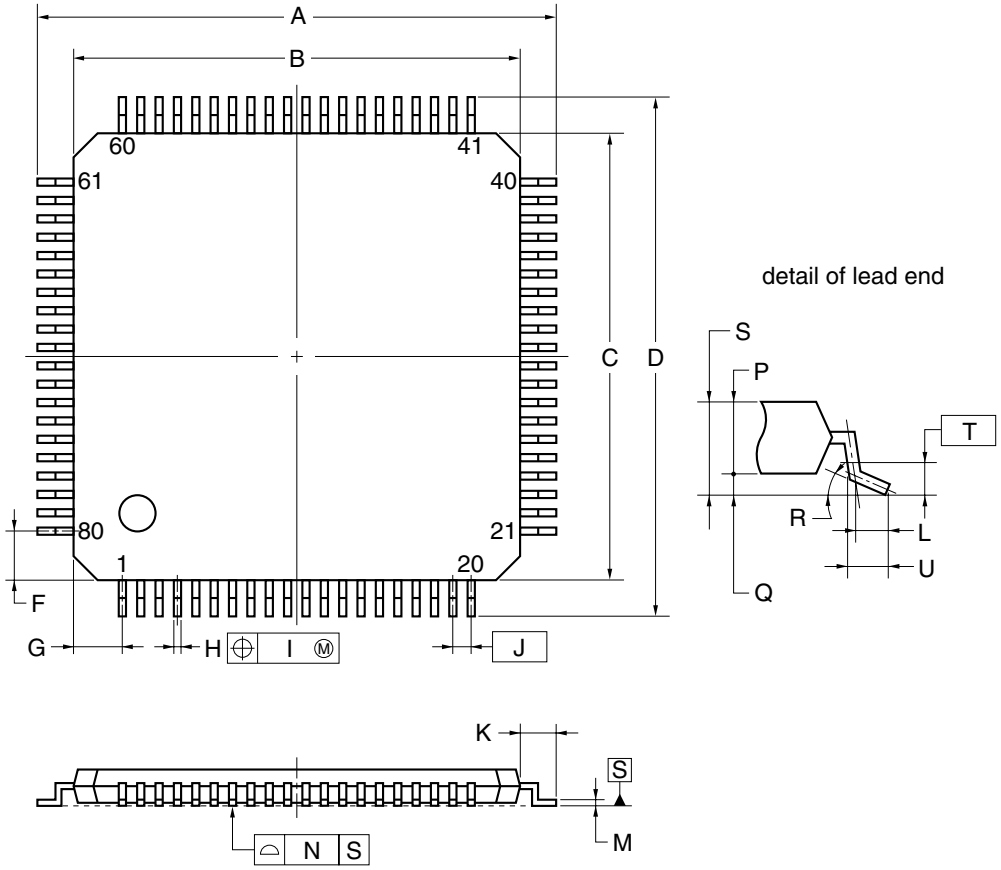
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

★ 80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.145±0.05
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P80GK-50-9EU-1

14. RECOMMENDED SOLDERING CONDITIONS

The μPD789405A, 789406A, 789407A, 789415A, 789416A, and 789417A should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions (1/2)

μPD789405AGC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD789406AGC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD789407AGC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD789415AGC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD789416AGC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD789417AGC-×××-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Condition	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less	VP15-00-2
Wave soldering	Soldering bath temperature: 260°C max., Time: 10 seconds max., Count: 1, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

Table 14-1. Soldering Conditions for Surface Mount Type (2/2)

μPD789405AGK-×××-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD789406AGK-×××-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD789407AGK-×××-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD789415AGK-×××-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD789416AGK-×××-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD789417AGK-×××-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
★ Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours).	IR35-107-2
★ VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours).	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C, 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for development of a system using the μPD789405A, 789406A, 789407A, 789415A, 789416A, or 789417A.

Language processor software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789418[Notes 1, 2, 3]	Device file for μPD789407A and 789417A Subseries

Flash memory writing tools

FlashproIII (FL-PR3[Note 4], PG-FP3)	Flash programmer for on-chip flash memory microcontrollers
★ FA-80GC-8BT[Note 4]	Flash memory writing adapter for 80-pin plastic QFP (GC-8BT type)
FA-80GK-9EU[Note 4]	Flash memory writing adapter for 80-pin plastic TQFP (fine pitch) (GK-9EU type)

Debugging tools

IE-78K0S-NS In-circuit emulator		In-circuit emulator for debugging the hardware and software when application systems which use the 78K/0S Series are developed. Supports the integrated debugger (ID78K0S-NS). Used with an AC adapter, emulation probe, and interface adapter that connects the host machine.
IE-70000-MC-PS-B AC adapter		Adapter used to supply power from a 100 to 240 V AC outlet.
IE-70000-98-IF-C Interface adapter		Adapter necessary when using a PC-9800 series (except notebook PC) as the host machine for the IE-78K0S-NS (C bus supported).
IE-70000-CD-IF-A PC card interface		PC card and interface cable necessary when a notebook PC is used as the host machine of the IE-78K0S-NS (PCMCIA socket supported).
IE-70000-PC-IF-C Interface adapter		Adapter necessary when an IBM PC/AT™ or compatible machine is used as the host machine for the IE-78K0S-NS (ISA bus supported).
★ IE-70000-PCI-IF-A Interface adapter		Adapter necessary when using a PC with a PCI bus as the host machine for the IE-78K0S-NS.
IE-789418-NS-EM1 Emulation board		Board for emulating device-specific peripheral hardware. This is used in combination with an in-circuit emulator.
★ NP-80GC[Note 4] Emulation probe		Cable to connect an in-circuit emulator to the target system. This is used in combination with the EV-9200GC-80.
	EV-9200GC-80 Conversion socket	Conversion socket to connect the NP-80GC to a target system board on which an 80-pin plastic QFP (GC-8BT type) can be mounted.
★ NP-80GC-TQ[Note 4] Emulation probe		Cable to connect an in-circuit emulator to the target system. This is used in combination with the TGC-080SBP.
	TGC-080SBP[Note 5] Conversion adapter	Conversion socket to connect the NP-80GC-TQ to a target system board on which an 80-pin plastic QFP (GC-8BT type) can be mounted.
★ NP-80GK[Note 4] Emulation probe		Cable to connect an in-circuit emulator to the target system. This is used in combination with the TGK-080SDW.
	TGK-080SDW[Note 5] Conversion adapter	Conversion socket to connect the NP-80GK to a target system board on which an 80-pin plastic TQFP (GK-9EU type) can be mounted.
SM78K0S[Notes 1, 2]		System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]		Integrated debugger common to 78K/0S Series
DF789418[Notes 1, 2]		Device file for μPD789407A and 789417A Subseries

Real-time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes 1. PC-9800 series (Japanese Windows™) based

2. IBM PC/AT or compatibles (Japanese/English Windows) based

3. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based

4. These are products of Naito Densei Machida Mfg. Co., Ltd. (Tel: 044-822-3813).

5. These are products made by TOKYO ELETECH CORPORATION.
For further information, contact: Daimaru Kogyo, Ltd.
Tokyo Electronic Division (+81-3-3820-7112)
Osaka Electronic Division (+81-6-6244-6672)

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789418.

APPENDIX B. RELATED DOCUMENTS

The related documents indicated to in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD789405A, 789406A, 789407A, 789415A, 789416A, 789417A Data Sheet	This document
μPD78F9418A Data Sheet	U14595E
μPD789407A, 789417A Subseries User's Manual	U13952E
78K/0S Series Instructions User's Manual	U11047E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U11622E
	Language	U11599E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U11816E
	Language	U11817E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or later	External Part User Open Interface Specifications	To be prepared
ID78K0-NS,ID78K0S-NS Integrated Debugger Ver. 2.20 or later Windows Based	Operation	U14910E
IE-78K0S-NS In-Circuit Emulator		U13549E
IE-789418-NS-EM1 Emulation Board		U14364E

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0S Series OS MX78K0S	Fundamental	U12938E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products & Packages - (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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