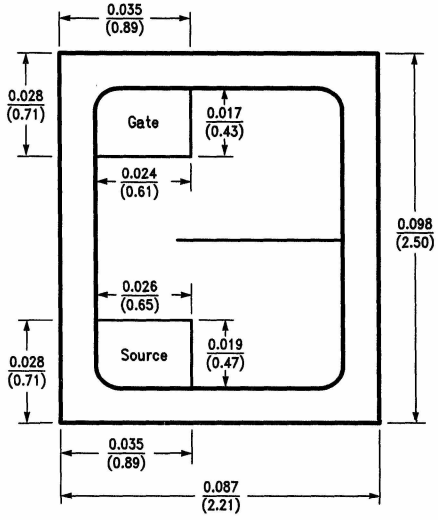
National Semiconductor

# Process A3
# N-Channel Power MOSFET




TL/G/10040–27

**DESCRIPTION**

These dice are n-channel, enhancement mode, power MOSFETs designed especially for high power, high speed applications, such as power supplies, AC and DC motor control and high energy pulse circuits.

This process is available in the following device types:

TO-220 (Case 37)

IRF710

IRF711

IRF712

IRF713

MTP2N35

MTP2N40

## Electrical Characteristics $T_C$ = 25°C (unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage (Note 1) | $I_D$ = 250 μA; $V_{GS}$ = 0V | 400 | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain | $V_{DS}$ = Rated Voltage<br>$V_{GS}$ = 0V | | 250 | μA |
| $I_{GSS}$ | Gate Leakage Current | $V_{DS}$ = ±20V; $V_{DS}$ = 0V | | 100 | nA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $I_D$ = 250 μA; $V_{DS}$ = $V_{GS}$ | 2.0 | 4.0 | V |
| $R_{DS(ON)}$ | Static On-Resistance (Note 2) | $V_{GS}$ = 10V; $I_D$ = 2.0A | | 3.6 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10V; $I_D$ = 2.0A | 0.5 | | Siemens |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25V; $V_{GS}$ = 0V<br>f = 1 MHz | | 200 | pF |
| $C_{oss}$ | Output Capacitance | | | 50 | pF |
| $C_{rss}$ | Reverse Transfer | | | 15 | pF |
| $t_{d(on)}$ | Turn-On Delay Time (Note 3) | $V_{DD}$ = 200V; $I_D$ = 0.8A<br>$V_{GS}$ = 10V; $R_{GEN}$ = 50Ω | | 10 | ns |
| $t_r$ | Rise Time | $R_{GS}$ = 50Ω | | 20 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 10 | ns |
| $t_f$ | Fall Time | | | 15 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 10V; $I_D$ = 2.0A<br>$V_{DD}$ = 200V | | 7.5 | nC |

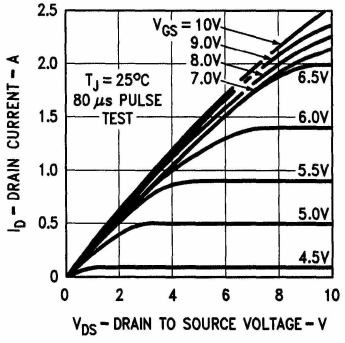
**Note 1:** $T_J$ = +25°C to +150°C.

**Note 2:** Pulse Test: Pulse Width ≤ 80 μs, Duty Cycle ≤ 1%.

**Note 3:** Switching time measurements performed on LEM TR-58 test equipment.

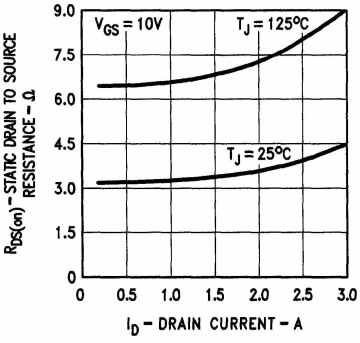
# Process A3

## Typical Performance Characteristics



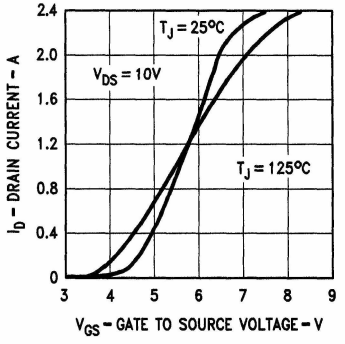

TL/G/10040–28

**FIGURE 1. Output Characteristics**



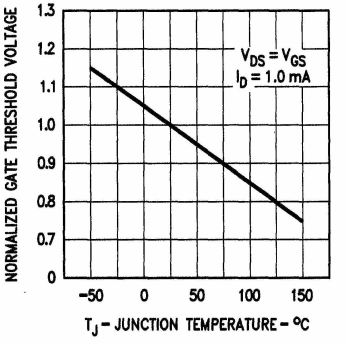

TL/G/10040–29

**FIGURE 2. Static Drain to Source Resistance vs Drain Current**



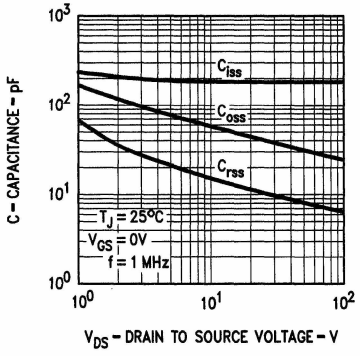

TL/G/10040–30

**FIGURE 3. Transfer Characteristics**



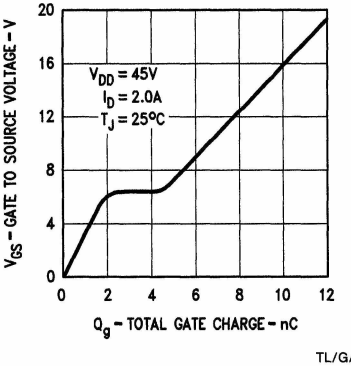

TL/G/10040–31

**FIGURE 4. Temperature Variation of Gate to Source Threshold Voltage**




TL/G/10040–32

**FIGURE 5. Capacitance vs Drain to Source Voltage**

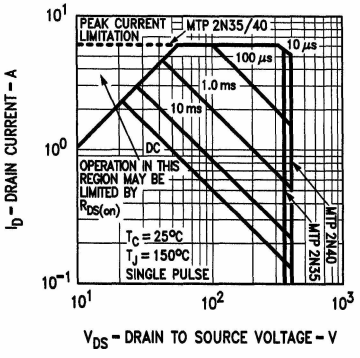



TL/G/10040–33

**FIGURE 6. Gate to Source Voltage vs Total Gate Charge**

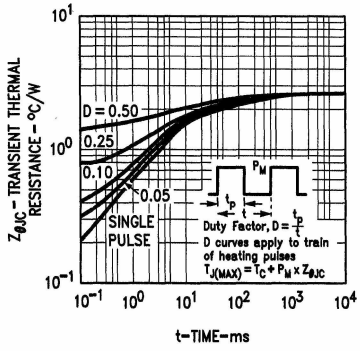
Process A3

## Typical Performance Characteristics (Continued)



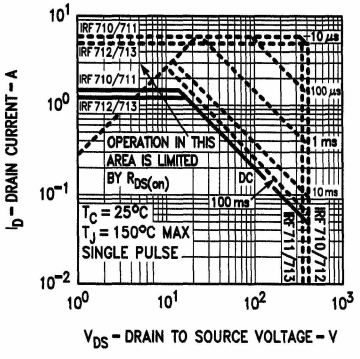

TL/G/10040-34

**FIGURE 7. Forward Biased Safe Operating Area for MTP2N35/2N40**



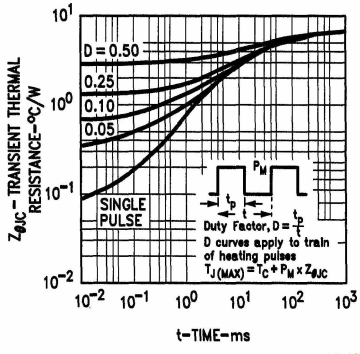

TL/G/10040-35

**FIGURE 8. Transient Thermal Resistance vs Time for MTP2N35/2N40**




TL/G/10040-36

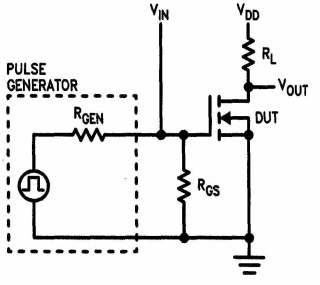
**FIGURE 9. Forward Biased Safe Operating Area for IRF710–713**




TL/G/10040-37

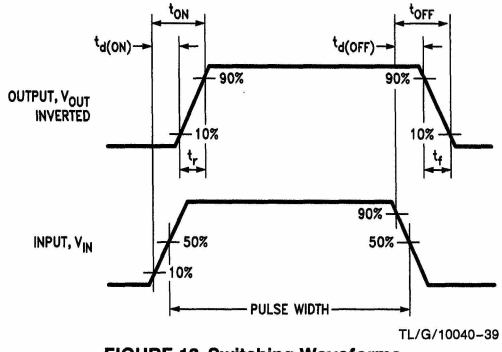
**FIGURE 10. Transient Thermal Resistance vs Time for IRF710–713**

## Typical Electrical Characteristics




TL/G/10040-38

**FIGURE 11. Switching Test Circuit**




TL/G/10040-39

**FIGURE 12. Switching Waveforms**