SGS-THOMSON MICROELECTRONICS

SGSP301 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

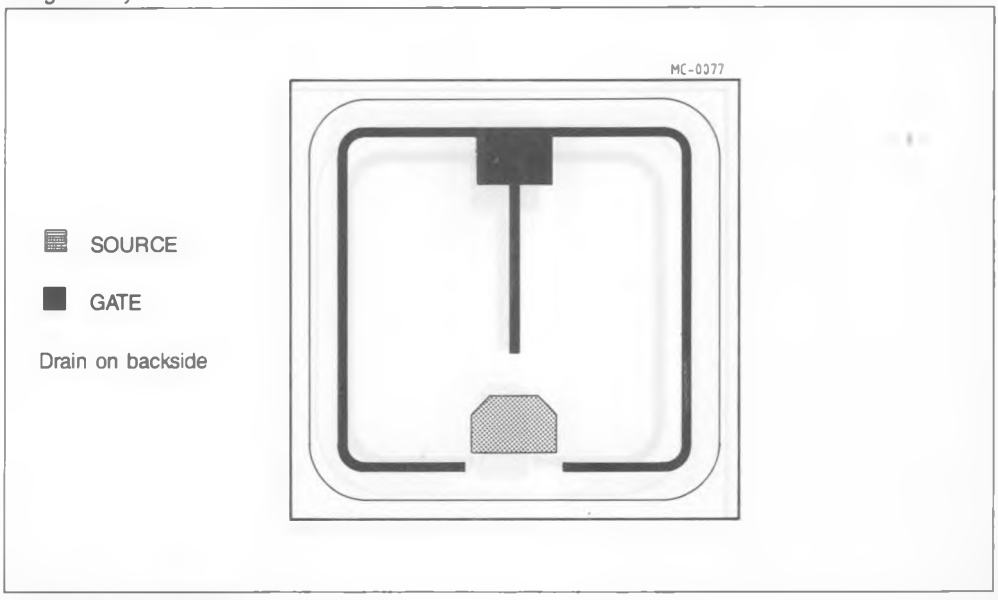
- DIE SIZE: 52 x 53 mils
- METALLIZATION:
  - Top: Al
  - Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  - Source: 4.4 x 6.5 mils
  - Gate: 4.4 x 6.5 mils
- RECOMMENDED WIRE BONDING:
  - Source: Au - max 2 mils
  - Gate: Au - max 2 mils

SCHEMATIC DIAGRAM

V_{DSS}	$R_{DS\ (on)}$	I_D*
100 V	1.4 Ω	2.0 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 6.95°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			±100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			1.4	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet