

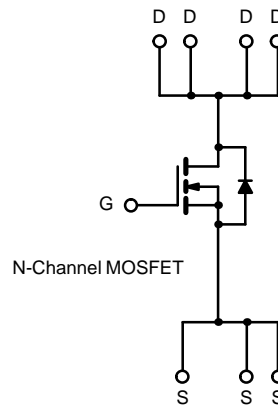
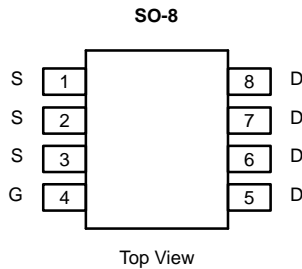


N-Channel 30-V (D-S) MOSFET

New Product

TrenchFET[®]
Power MOSFETs
High-Efficiency
PWM Optimized

PRODUCT SUMMARY		
V _{DS} (V)	R _{DS(ON)} (Ω)	I _D (A)
30	0.0135 @ V _{GS} = 10 V	± 10
	0.020 @ V _{GS} = 4.5 V	± 8



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	± 10
		T _A = 70 °C	± 8
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	± 50	A
Continuous Source Current (Diode Conduction) ^a	I _S	2.3	
Maximum Power Dissipation	P _D	T _A = 25 °C	2.5
		T _A = 70 °C	1.6
Operating Junction and Storage Temperature Range (MOSFET and Schottky)	T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient (MOSFET) ^a	R _{thJA}	t ≤ 10 seconds	50	°C/W
		Steady State	70	

Notes
A. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70806.



MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		0.0105	0.0135	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$		0.0155	0.020	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 10 \text{ A}$		28		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.3 \text{ A}, V_{GS} = 0 \text{ V}$		0.74	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		37	60	nC
Gate-Source Charge	Q_{gs}			8		
Gate-Drain Charge	Q_{gd}			7		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15 \text{ V}, R_L = 15 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		15	30	ns
Rise Time	t_r			8	15	
Turn-Off Delay Time	$t_{d(off)}$			45	90	
Fall Time	t_f			18	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		50	80	

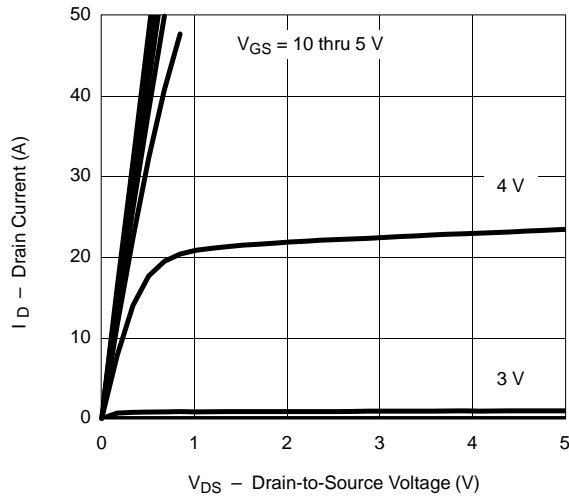
Notes

- A. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 B. Guaranteed by design, not subject to production testing.

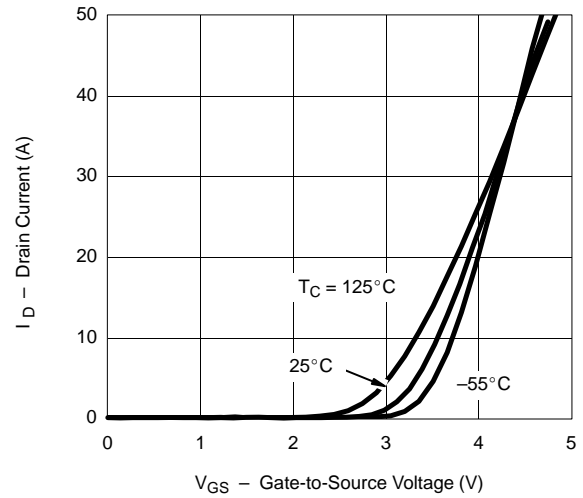


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

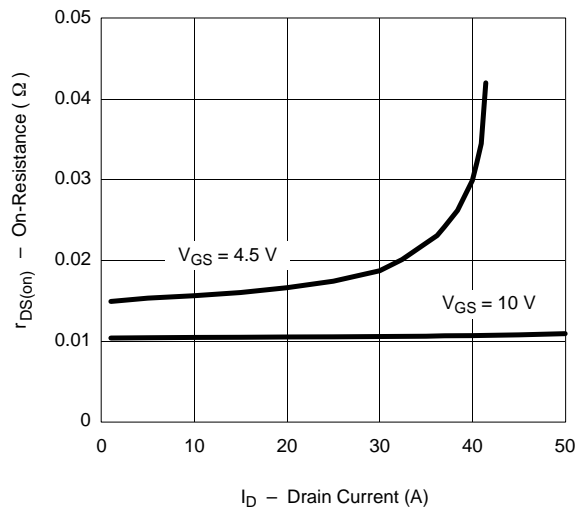
Output Characteristics



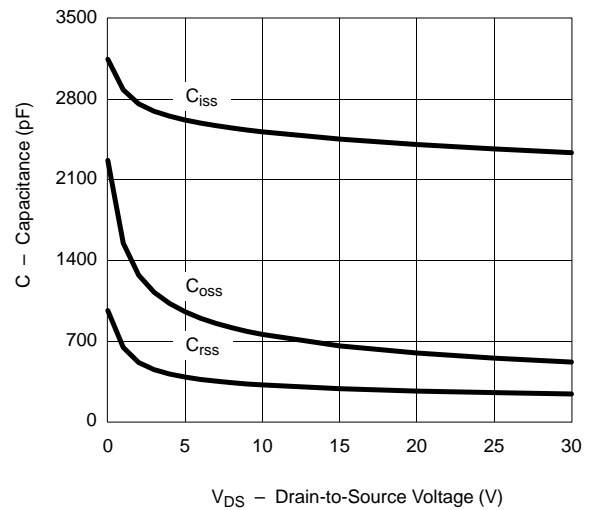
Transfer Characteristics



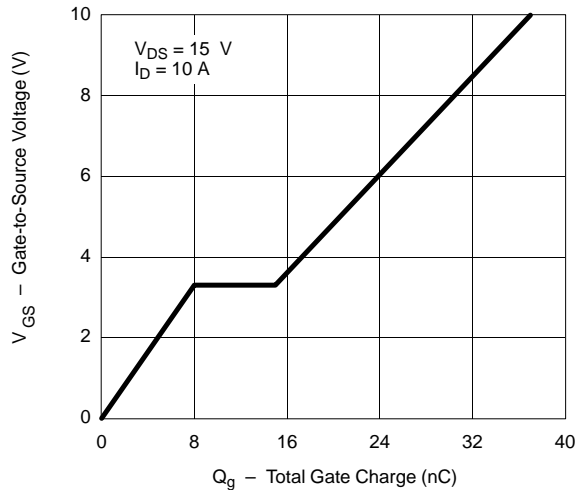
On-Resistance vs. Drain Current



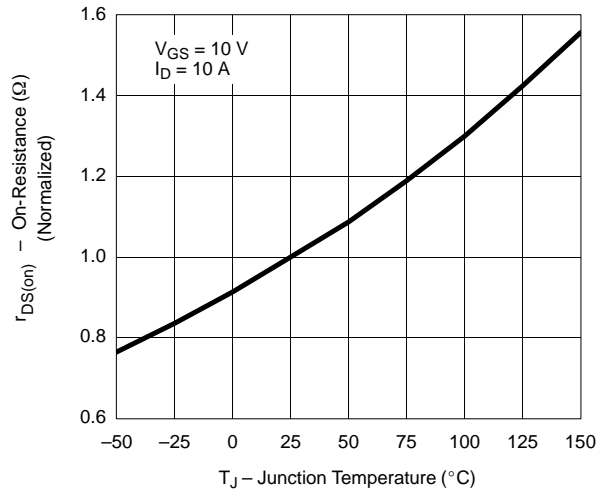
Capacitance



Gate Charge

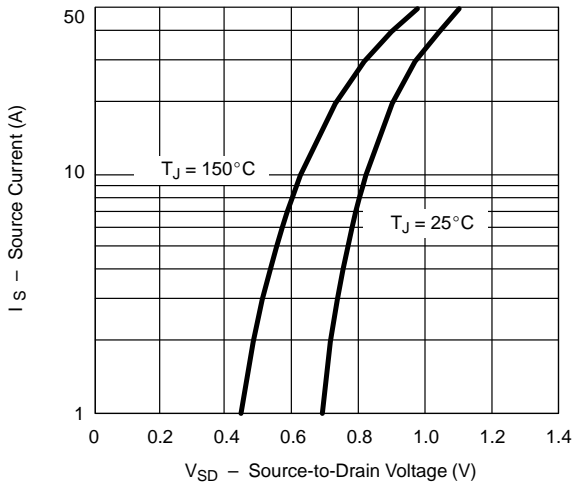


On-Resistance vs. Junction Temperature

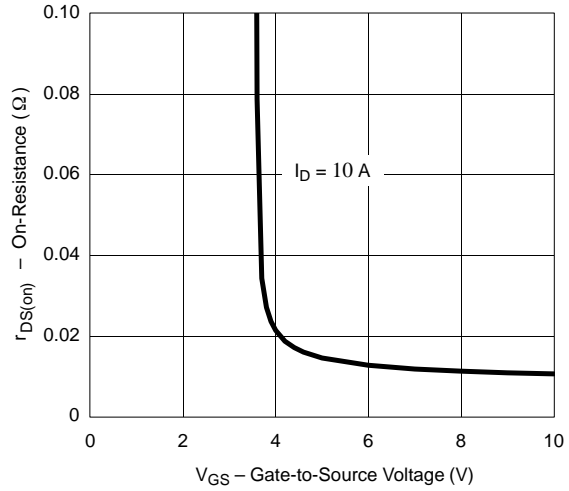


TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

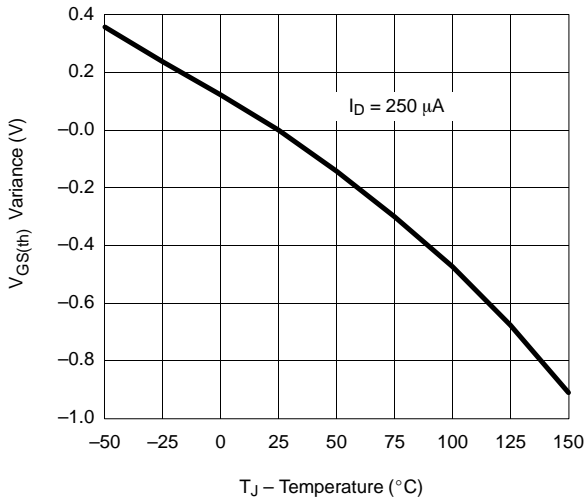
Source-Drain Diode Forward Voltage



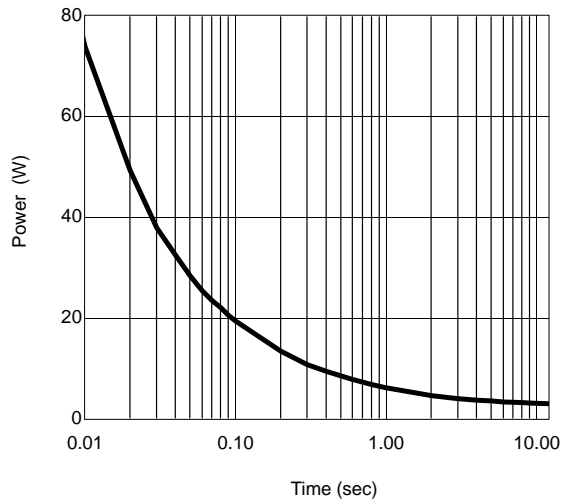
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

