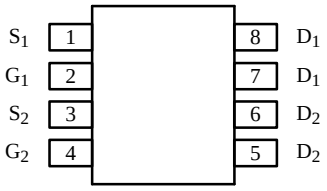
Dual N-Channel Enhancement-Mode MOSFET

Product Summary

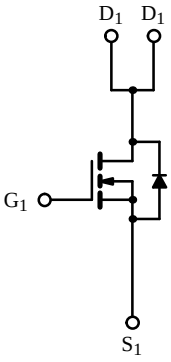
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.05 @ V_{GS} = 4.5 V	± 5.0
	0.06 @ V_{GS} = 3.0 V	± 4.2
	0.08 @ V_{GS} = 2.5 V	± 3.6

Recommended upgrade: Si9926DY

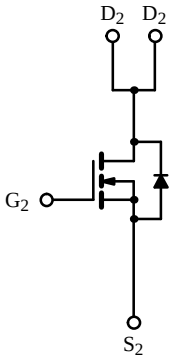
SO-8



Top View



N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 5.0	A
	T_A = 70°C		± 4.0	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	± 48	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1227. A SPICE Model data sheet is available for this product (FaxBack document #5130).

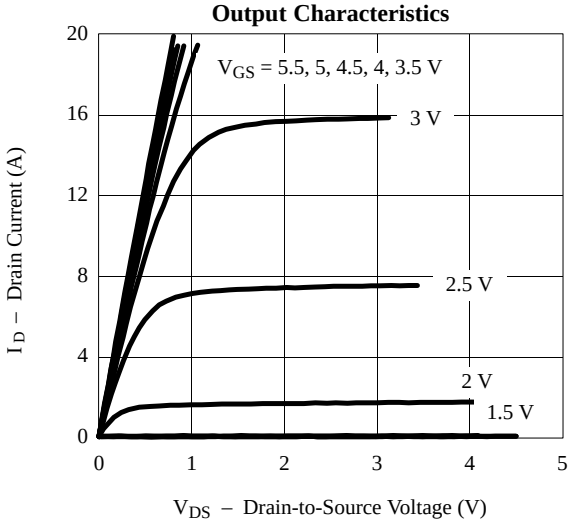
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.8			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V			1	µA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 70°C			5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 5 V	10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 7.2 V, I_D = 5.0 A	0.025	0.036	0.045	Ω
		V_{GS} = 4.5 V, I_D = 5.0 A		0.041	0.05	
		V_{GS} = 3.0 V, I_D = 3.9 A		0.050	0.07	
		V_{GS} = 2.5 V, I_D = 1 A		0.060	0.08	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 5.0 A		13		S
Diode Forward Voltage[b]	V_{SD}	I_S =5.0 A, V_{GS} = 0 V		0.9	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 5.0 A		10	20	nC
Gate-Source Charge	Q_{gs}			2.6		
Gate-Drain Charge	Q_{gd}			3.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 6 V, R_L = 6 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		13	40	ns
Rise Time	t_r			9	30	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	t_f			9	30	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 5.0 A, di/dt = 100 A/µs		100	150	

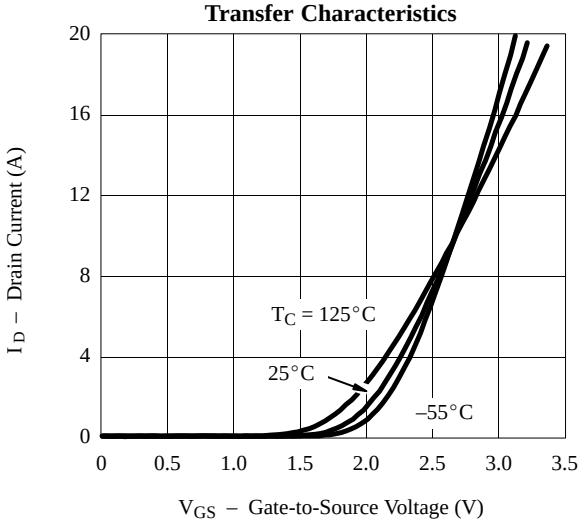
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

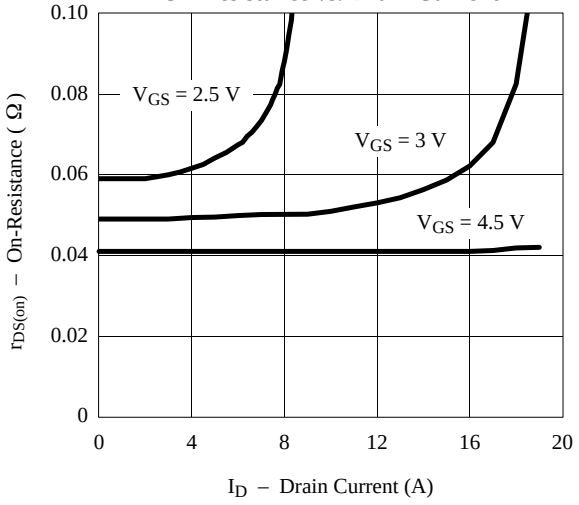
Output Characteristics



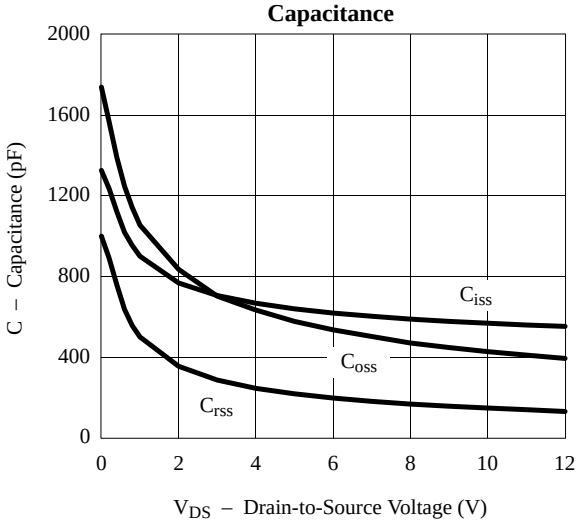
Transfer Characteristics



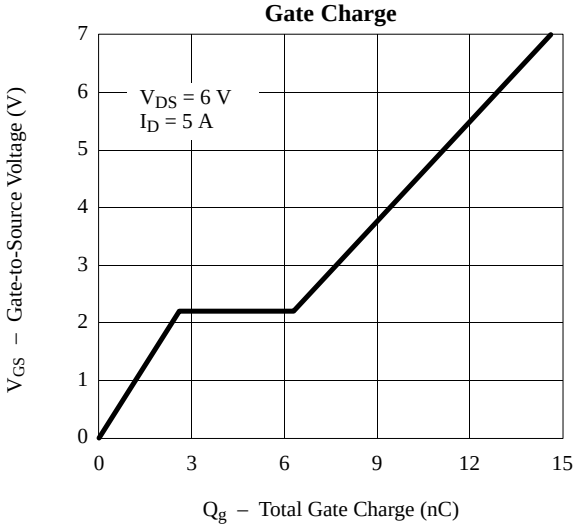
On-Resistance vs. Drain Current



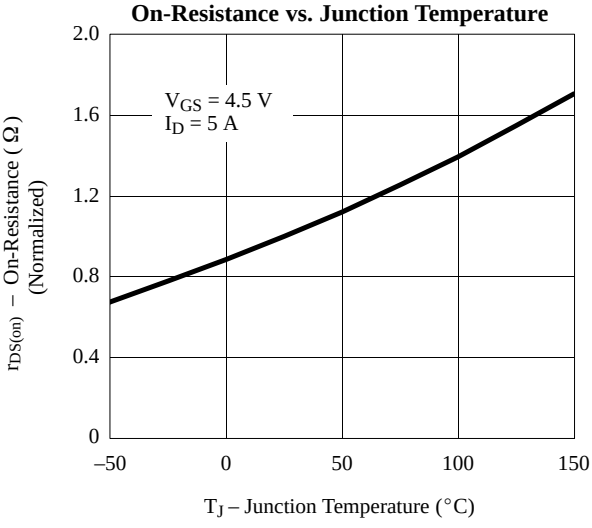
Capacitance



Gate Charge

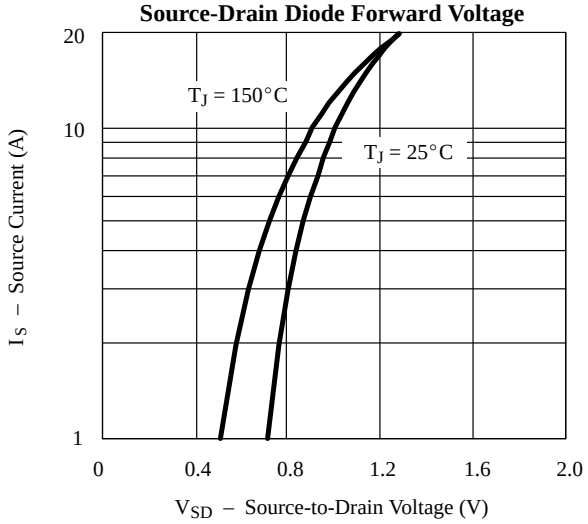


On-Resistance vs. Junction Temperature

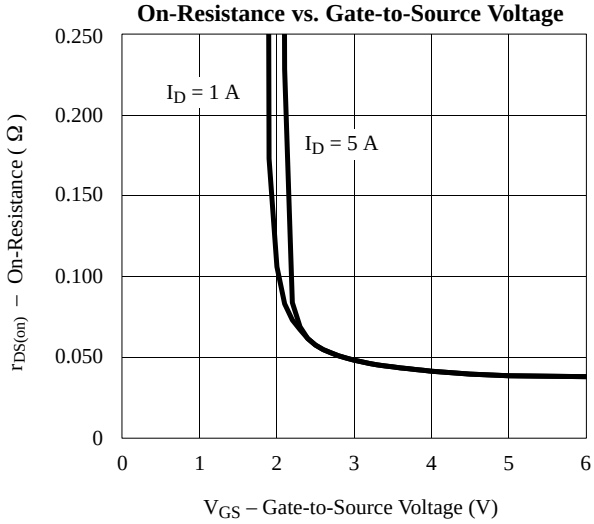


Typical Characteristics (25°C Unless Otherwise Noted)

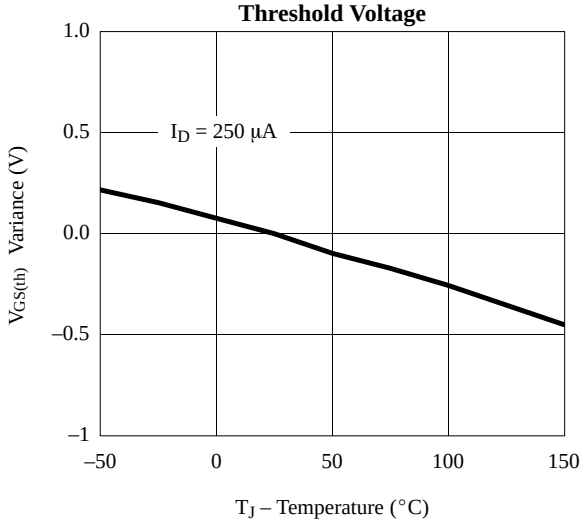
Source-Drain Diode Forward Voltage



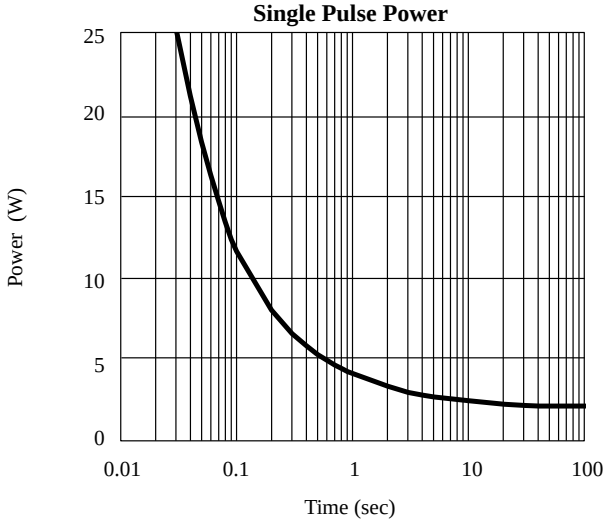
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient