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High Power Silicon Controlled Rectifier 1300 Volts 235 A RMS

C180

AMPLIFYING GATE

C180 Silicon Controlled Rectifier is designed for phase control applications. This is an all-diffused Pic-Pac device, employing the field-proven amplifying gate.

FEATURES:

- High di/dt Ratings
- High dv/dt Capability with Selections Available
- Excellent Surge and I2t Ratings Providing Easy Fusing
- Rugged Hermetic Package with Long Creepage Path



ТҮРЕ	REPETITIVE PEAK OFF-STATE VOLTAGE, V _{DRM} T _J = -40°C to +125°C	REPETITIVE PEAK REVERSE VOLTAGE, V _{RRM} ¹ T _J = -40°C to +125°C	NON-REPETITIVE PEAK REVERSE VOLTAGE, V _{RSM} T _J = +125°C 200 Volts	
C180A	100 Volts	100 Volts		
C180B	200	200	300	
C180C	300	300	400	
C180D	400	400	500	
C180E	500	500	600	
C180M	600	600	720	
C180S	700	700	840	
C180N	800	800	950	
C180T	900	900	1075	
C180P	1000	1000	1200	
C180PA	1100	1100	1325	
C180PB	1200	1200	1450	
C180PC	1300	1300	1550	

¹ Half sinewave waveform, 10 msec. max. pulse width.

RMS On-State Current, I _{T(RMS)}
Average On-State Current, $I_{T(AV)}$
Peak One-Cycle Surge (Non-Repetitive) On-State Current, I _{TSM} (60 Hz)
Peak One-Cycle Surge (Non-Repetitive) On-State Current, I _{TSM} (50 Hz)
Critical Rate-of-Rise of On-State Current (Non-Repetitive)*
Critical Rate-of-Rise of On-State Current (Repetitive)*
12t (for fusing) for times ≥ 1.5 milliseconds
Peak Gate Power Dissipation, Power and Power Dissipation and Power Dissipation Power
Average Cate Power Dissination Power
Chance Townspoture T
Operating Temperature, T _J
Stud Torque
Stud Torque

Quality Semi-Conductors

CHARACTERISTICS

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Repetitive Peak Reverse					mA	$T_I = +25$ °C
and Off-State Current	I _{DRM}	ĺ		l		•
	IRRM					$V_{DRM} = V_{RRM} =$
C180A	[-	3	10	1	100 Volts Peak
C180B	İ İ		3	10		200
C180C	1		3	10	į	300
C180D	i i		3	10	Į	400
C180E	1]		3	10	[500
C180M	1		3	10	[600
C180S	1		3	10		700
C180N	1		3	10		800
C180T	1		3	9		900
C180P	1		3	7		1000
C180PA	1 !	-	3	7		1100
C180PB	1	-	3	6	1	1200
C180PC	1 '		3	5		1300
Repetitive Peak Reverse	I _{DRM}				mA	$T_{J} = +125^{\circ}C$
and Off-State Current	and					V _{DRM} = V _{RRM} =
C1004	IRRM		15	20		100 Volts Peak
C180A	4		15	20		200
C180B	4		15	20	!	300
C180C	-		15	20	1	400
C180D	-{		15	$\frac{20}{20}$	1	500
C180E	4		15	20		600
C180M	4		15	20	{	700
C180S	4			$\frac{20}{20}$	1	800
C180N	4	ļ. -	15	18	-	900
C180T	4		15	15	-	1000
C180P	4	<u> </u>	12		ł	1100
C180PA	4	<u> </u>	11	14	ł	1200
C180PB	4		10	$\frac{13}{11}$	4	1300
C180PC	.l	-	8		0000	Junction-to-Case
Thermal Resistance	$R_{\theta JC}$.12	.14	°C/Watt	
Critical Rate-of-Rise of Off-State Voltage. (Higher values may cause device switching.)	dv/dt	200	500	-	V/μsec	$T_I = +125^{\circ}$ C, $V_{DRM} = Rated$ Using Linear or Exponential Rising Waveform, Gate Open Circuited. Exponential dv/dt = (.632)
	High	er minim	um dv/dt	selections :	available —	consult factory.
Holding Current	I _H	T -	75	500	mAdc	T _C = +25°C, Anode Supply = 24 Vdc. Initial On-State Current - 2.5 Amps.
Turn-On Delay Time	t _đ	-	1		µsec	T _C = +25°C, I _T = 100 Adc, V _{DRM} = Rated Gate Supply: 10 Volt Open Circuit, 25 Ohm, 0.1 μsec max. rise time.
Gate Pulse Width Necessary to Trigger		-	8	10	µsec	$T_C = 25$ °C, Gate Supply: 20 Volt Open Circuit, 40 Ohm, .5 μ sec rise time. $I_T = 1$ Amp. For High di/dt Capability, See Chart 7.
DC Gate Trigger Current	I_{GT}	-	100	150	mAdc	$T_C = +25^{\circ}C, V_D = 6 \text{ Vdc}, R_L = 3 \text{ Ohms}$
20 0000 11.0800 00000000	-0.		 	200	7	$T_C = -40^{\circ}C, V_D = 6 \text{ Vdc}, R_L = 3 \text{ Ohms}$
	l	 	 	125	7	$T_C = +125$ °C, $V_D = 6$ Vdc, $R_L = 3$ Ohms
DC Gate Trigger Voltage	V _{GT}	-	1.25	3.0	Vdc	$T_C = -40^{\circ}\text{C to } +125^{\circ}\text{C}, V_D = 6 \text{ Vdc}, R_L = 3 \text{ Ohms}$
	}	0.15	-	 	7	$T_C = +125$ °C, $V_D = Rated$, $R_L = 1000$ Ohms
Peak On-State Voltage	V _{TM}	-	2.3	2.85	Volts	T _C = +25°C, I _{TM} = 1500 Amps. Peak Duty Cycle ≤ 0.01%