



# **Phase Control Thyristor**

Replaces August 2000 version, DS4652-4.1

DS4652-5.1 November 2002

#### **PACKAGE OUTLINE**

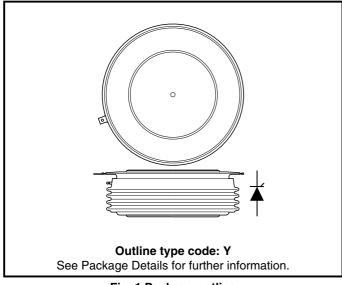


Fig. 1 Package outline

#### **KEY PARAMETERS**

 $\begin{array}{lll} {\rm V_{DRM}} & 1200 {\rm V} \\ {\rm I_{T(AV)}} & 4135 {\rm A} \\ {\rm I_{TSM}} & 64000 {\rm A} \\ {\rm dVdt^*} & 1000 {\rm V/\mu s} \\ {\rm dI/dt} & 500 {\rm A/\mu s} \\ \end{array}$ 

\*Higher dV/dt selections available

#### **VOLTAGE RATINGS**

Part Number	Repetitive Peak Voltages V <sub>DRM</sub> V <sub>RRM</sub>	Conditions
	v	
DCR1473SY12	1200	$\begin{split} &T_{vj}=0^{\circ} \text{ to } 125^{\circ}\text{C.} \\ &I_{DRM}=I_{RRM}=250\text{mA.} \\ &V_{DRM}, V_{RRM}=10\text{ms } 1/2 \text{ sine.} \\ &V_{DSM} \& V_{RSM}=V_{DRM} \& V_{RRM}+100V \\ &\text{respectively.} \end{split}$

Lower voltage grades available.

#### **ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

If a lower voltage grade is required, then use  $V_{\tiny DRM}/100$  for the grade required e.g.:

DCR1473SY08 for an 800V variant etc.

Note: Please use the complete part number when ordering and quote this number in any future correspondance relating to your order.



## **CURRENT RATING**

 $T_{case} = 60^{\circ}C$  unless stated otherwise.

Symbol	Parameter	Conditions	Max.	Units				
Double Sic	Double Side Cooled							
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	4135	Α				
I <sub>T(RMS)</sub>	RMS value	-	6495	Α				
I <sub>T</sub>	Continuous (direct) on-state current	-	5700	Α				
Single Side Cooled (Anode side)								
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	2605	Α				
I <sub>T(RMS)</sub>	RMS value	-	4090	Α				
I <sub>T</sub>	Continuous (direct) on-state current	-	3290	Α				

## **CURRENT RATING**

T<sub>case</sub> = 80°C unless stated otherwise.

Symbol	Parameter	Conditions	Max.	Units			
Double Sic	Double Side Cooled						
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	3190	Α			
I <sub>T(RMS)</sub>	RMS value	-	5010	А			
I <sub>T</sub>	Continuous (direct) on-state current	-	3950	Α			
Single Side	Single Side Cooled (Anode side)						
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	1966	А			
I <sub>T(RMS)</sub>	RMS value	-	3090	Α			
I <sub>T</sub>	Continuous (direct) on-state current	-	2410	Α			



## **SURGE RATINGS**

Symbol	Parameter	Conditions	Max.	Units
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine; T <sub>case</sub> = 125°C	51.0	kA
l²t	I <sup>2</sup> t for fusing	V <sub>R</sub> = 50% V <sub>RRM</sub> - 1/4 sine	13.1x 10 <sup>6</sup>	A²s
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine; T <sub>case</sub> = 125°C	64.0	kA
l²t	I <sup>2</sup> t for fusing	V <sub>R</sub> = 0	20.48 x 10 <sup>6</sup>	A²s

#### THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
R <sub>th(j-c)</sub>	Thermal resistance - junction to case	Double side cooled	dc	-	0.0095	°C/W
		Single side cooled	Anode dc	-	0.019	°C/W
			Cathode dc	-	-	°C/W
R <sub>th(c-h)</sub>		Clamping force 43.0kN with mounting compound	Double side	-	0.002	°C/W
			Single side	-	0.004	°C/W
T <sub>vj</sub>	Virtual junction temperature	On-state (conducting)		-	135	°C
		Reverse (blocking)		-	125	°C
T <sub>stg</sub>	Storage temperature range			-55	125	°C
-	Clamping force			38.0	47.0	kN



## **DYNAMIC CHARACTERISTICS**

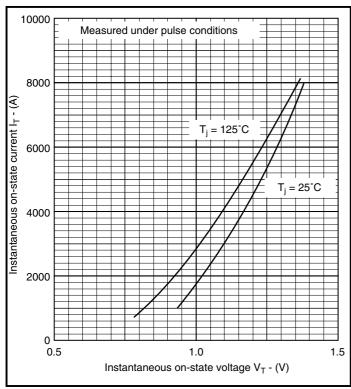
Symbol	Parameter	Conditions		Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C		250	mA
dV/dt	Maximum linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> T <sub>j</sub> = 125°C, gate open circuit		1000	V/μs
all/alk	dl/dt Rate of rise of on-state current	From 67% $V_{DRM}$ to 1000A Gate source 20V, 10 $\Omega$ $t_r = 0.5 \mu s$ to 1A, $T_j = 125 ^{\circ} C$	Repetitive 50Hz	250	A/μs
di/dt			Non-repetitive	500	A/μs
V <sub>T(TO)</sub>	Threshold voltage	At T <sub>vj</sub> = 125°C		0.824	V
r <sub>T</sub>	On-state slope resistance	At T <sub>vj</sub> = 125°C		0.066	mΩ
t <sub>gd</sub>	Delay time	$V_D = 67\%$ $V_{DRM}$ , Gate source 30V, 15Ω $t_r = 0.5\mu s$ , $T_j = 25$ °C		2.0	μs

## **GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	4.0	V
l <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	400	mA
$V_{\rm GD}$	Gate non-trigger voltage	At V <sub>DRM</sub> T <sub>case</sub> = 125°C	0.25	V
$V_{FGM}$	Peak forward gate voltage	Anode positive with respect to cathode	30	٧
$V_{FGN}$	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
$V_{RGM}$	Peak reverse gate voltage		5	V
I <sub>FGM</sub>	Peak forward gate current	Anode positive with respect to cathode	30	Α
$P_{G(PK)}$	Peak gate power	See Gate Characteristics curve/table	150	W
$P_{G(AV)}$	Mean gate power		10	W



## **CURVES**



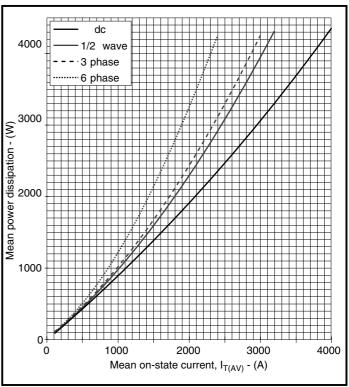


Fig. 2 Maximum (limit) on-state characteristics

Fig. 3 Power dissipation curves

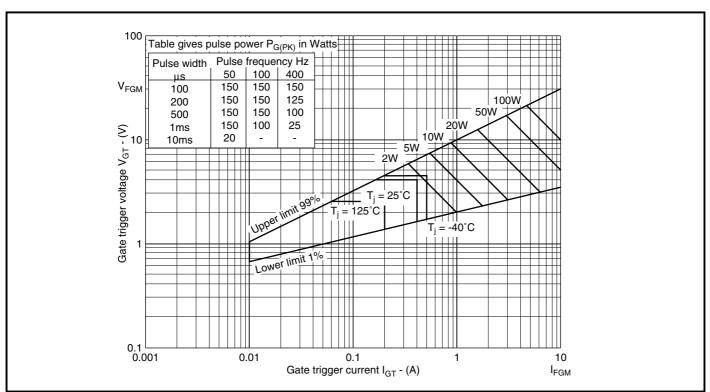


Fig. 4 Gate characteristics



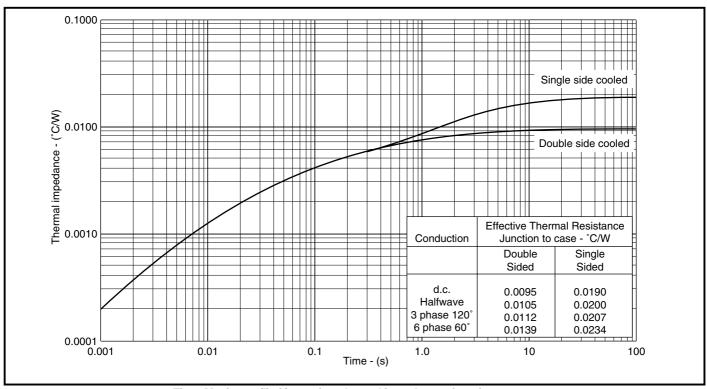


Fig. 5 Maximum (limit) transient thermal impedance - junction to case

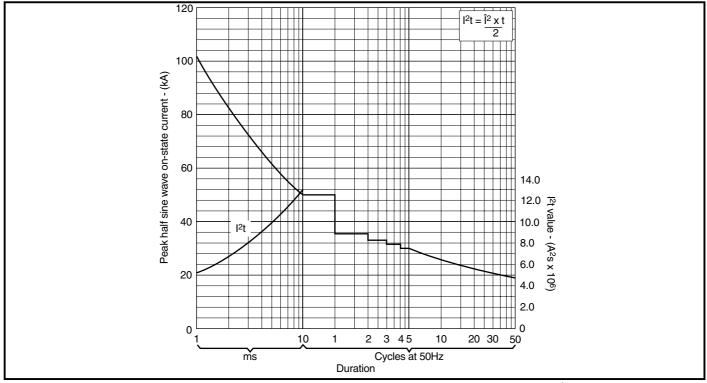


Fig. 6 Surge (non-repetitive) on-state current vs time (with 50%  $V_{RRM}$  at  $T_{case}$  = 125°C)



#### **PACKAGE DETAILS**

For more information please contact Customer Services. All dimensions are stated in mm unless stated otherwise. DO NOT SCALE.

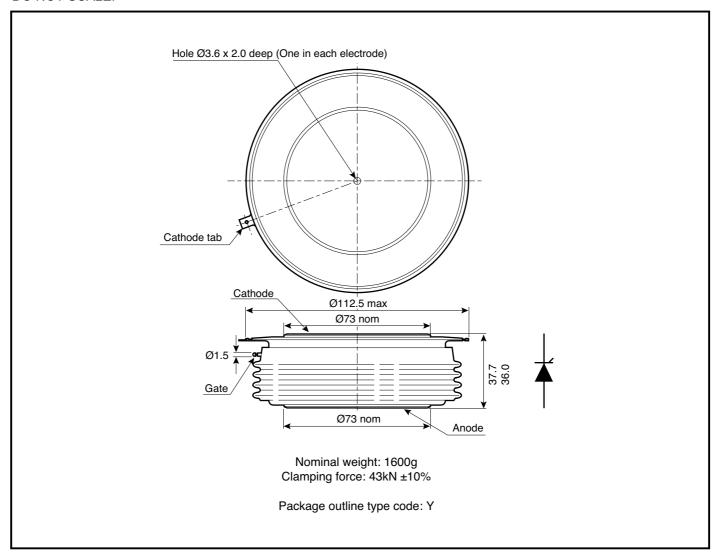


Fig. 7 Package outline



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The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

#### **HEATSINKS**

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.



http://www.dynexsemi.com

e-mail: power\_solutions@dynexsemi.com

HEADQUARTERS OPERATIONS

DYNEX SEMICONDUCTOR LTD

Deddington Bond Lincoln

Doddington Road, Lincoln. Lincolnshire. LN6 3LF. United Kingdom.

Tel: +44-(0)1522-500500 Fax: +44-(0)1522-500550 CUSTOMER SERVICE

Tel: +44 (0)1522 502753 / 502901. Fax: +44 (0)1522 500020

SALES OFFICES

Benelux, Italy & Switzerland: Tel: +33 (0)1 64 66 42 17. Fax: +33 (0)1 64 66 42 19.

France: Tel: +33 (0)2 47 55 75 52. Fax: +33 (0)2 47 55 75 59.

Germany, Northern Europe, Spain & Rest Of World: Tel: +44 (0)1522 502753 / 502901.

Fax: +44 (0)1522 500020

North America: Tel: (949) 733-3005. Fax: (949) 733-2986.

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