#### TOSHIBA THYRISTOR SILICON PLANAR TYPE

# **S6744**

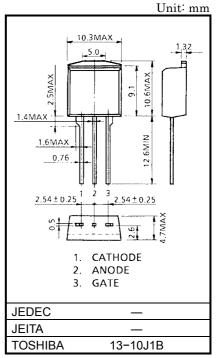
## MEDIUM POWER CONTROL APPLICATIONS

 Repetitive Peak Off-State Voltage : VDRM = 400V Repetitive Peak Reverse Voltage : VRRM = 400V
 Average On-State Current : IT (AV) = 8A

• A Large Current Pulse Capability

#### **MAXIMUM RATINGS**

CHARACTERISTIC	SYMBOL	RATING	UNIT	
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	$V_{ m DRM} \ V_{ m RRM}$	400	٧	
Non-Repetitive Peak Reverse Voltage (Non-Repetitive<5ms, $T_j = 0 \sim 125$ °C)	V <sub>RSM</sub>	500	٧	
Average On-State Current (Half Sine Waveform Tc = 72°C)	I <sub>T (AV)</sub>	8	Α	
R.M.S On-State Current	I <sub>T (RMS)</sub>	12.6	Α	
Peak One Cycle Surge On-State Current (Non-Repetitive)	I <sub>TSM</sub>	200 (50Hz)	А	
		220 (60Hz)		
I <sup>2</sup> t Limit Value	1 <sup>2</sup> t	200	A <sup>2</sup> s	
Repetitive Peak Surge On-State Current (Note 1)	I <sub>TRM</sub>	1300	А	
Critical Rate of Rise of On-State Current (Note 2)	di / dt	100	A/μs	
Peak Gate Power Dissipation	$P_{GM}$	5	W	
Average Gate Power Dissipation	P <sub>G</sub> (AV)	0.5	W	
Peak Forward Gate Voltage	$V_{FGM}$	10	V	
Peak Reverse Gate Voltage	$V_{RGM}$	-5	V	
Peak Forward Gate Current	I <sub>GM</sub>	2	Α	
Junction Temperature	Tj	-40~125	°C	
Storage Temperature Range	T <sub>stg</sub>	-40~125	°C	



Weight: 1.7 g

Note 1:  $C_M \le 500 \mu F$ ,  $t_W \le 300 \mu s$ ,  $V_D \le 350 V$ 

Note 2: di / dt Test condition

 $V_{DRM}$  = 0.5 × Rated,  $I_{TM} \le 25A$ ,  $t_{gw} \ge 10\mu s$ ,  $t_{gr} \le 250ns$ ,  $i_{gp} = I_{GT} \times 2.0$ 

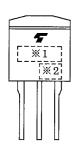
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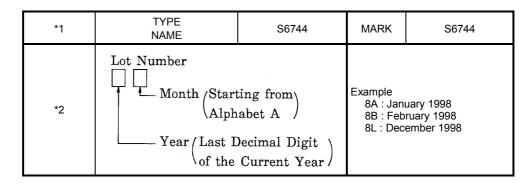


# **ELECTRICAL CHARACTERISTICS (Ta = 25°C)**

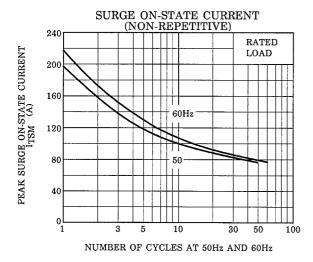
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse Current	I <sub>DRM</sub> I <sub>RRM</sub>	V <sub>DRM</sub> = V <sub>RRM</sub> = Rated	_	_	10	μΑ
Peak On-State Voltage	$V_{TM}$	I <sub>TM</sub> = 25A	_	_	1.5	V
Gate Trigger Voltage	V <sub>GT</sub>	$V_{\rm D} = 6V, R_{\rm I} = 10\Omega$	_	_	1.0	V
Gate Trigger Current	I <sub>GT</sub>	ν <sub>D</sub> = ον, τι <u>c</u> = τοιχ	_	_	20	mA
Gate Non-Trigger Voltage	$V_{GD}$	V <sub>D</sub> = Rated × 2 / 3, Tc = 125°C	0.2	_	_	V
Critical Rate of Rise of Off-State Voltage	dv / dt	V <sub>DRM</sub> = Rated,Tc = 125°C, Exponential Rise	_	50	_	V / µs
Holding Current	lΗ	V <sub>D</sub> = 6V, I <sub>TM</sub> = 1A	_	_	40	mA
Latching Current	ΙL	$V_D = 6V, f = 50Hz,$ $t_{gw} = 100\mu s, i_G = 40mA$	_	_	60	mA
Thermal Resistance	R <sub>th (j-a)</sub>	Junction to Ambient	_	_	70	°C/W

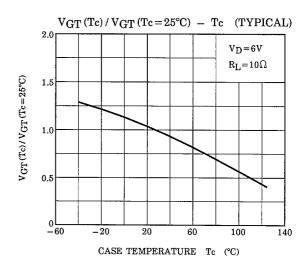
### **MARKING**

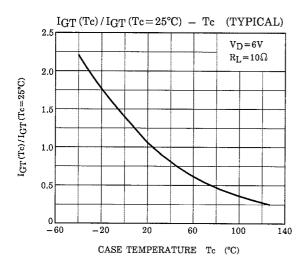


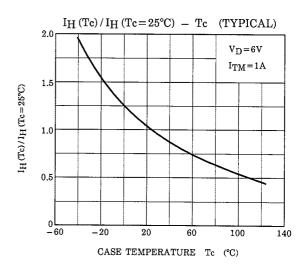


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