Mobile Pentium® Processor with MMX™ Technology on 0.25 Micron System Design Considerations

MHPG Technical Marketing

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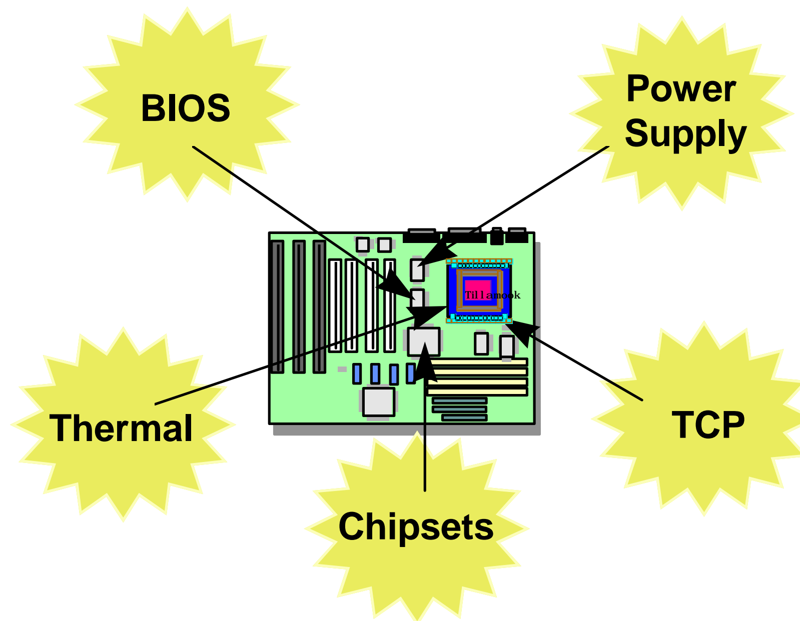
Topics

- **Overview and Differences Between Mobile Pentium(R) Processor with MMX™ Technology on 0.25 Micron**[1] (166/200/233/266 MHz) **and P55CLM**[2] (133/150/166 MHz)
- **Voltage Supply Solution**
- **Thermal Design Considerations**
- **I/O Signals**
- **Packaging**
- **Key Validation Areas**
- **Platform Readiness Summary**
- **Collateral**

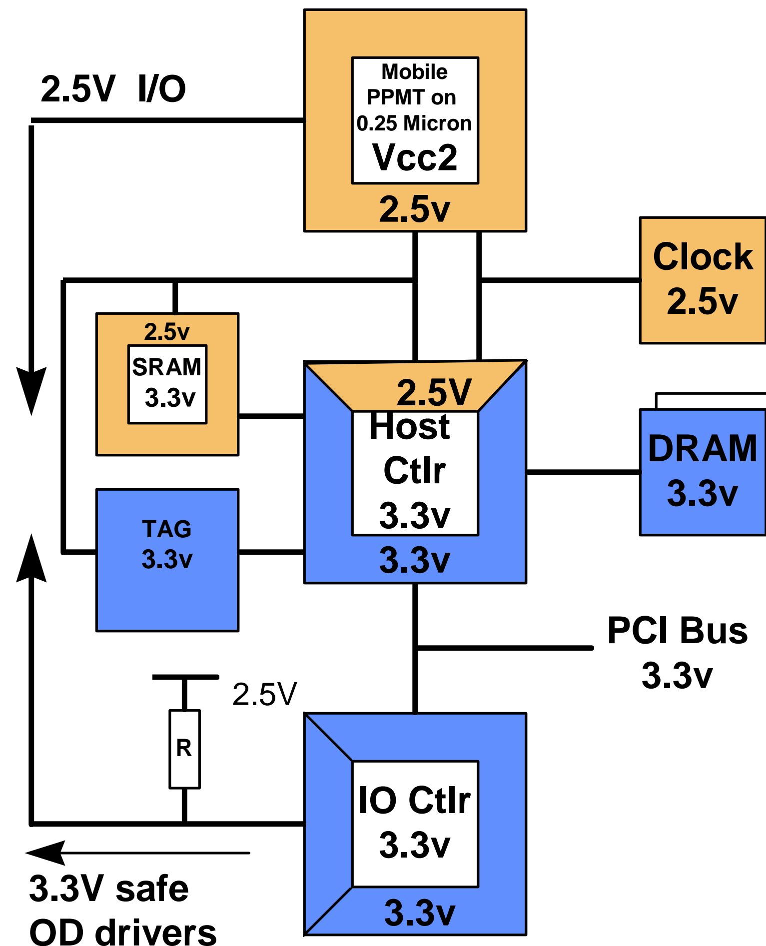
Notes:
1. Mobile PPMT on 0.25 Micron is Mobile Pentium(R) Processor with MMX(TM) Technology on 0.25 Micron
2. P55CLM is Mobile Pentium(R) Processor with MMX ™ Technology.

Overview

- **This presentation covers hardware design considerations for the Mobile Pentium(R) Processor with MMX™ Technology on 0.25 Micron at (166/200/233/266 MHz).**



Mobile Pentium(R) Processor with MMX™ Technology on 0.25 Micron Platform Block Diagram



Summary of Differences Between the Mobile Pentium(R) Processor with MMX™ Technology on 0.25 Micron and P55CLM

	P55CLM	Mobile PPMT on 0.25 Micron	OEM Impact
o Vcc2 (core)	2.45V + 0.215V /- 0.165V	1.8V ± 0.135V(166-233) 2.0V ± 0.150V(266)	Power Supply Design Re-qualification
o Vcc3 (I/O)	3.3V ± 5%	2.5V ± 5%	Power Supply Design Re-qualification
o Power Dissipation			
- TDP (max)	9.0W @ 166 MHz	7.6W @ 266 MHz	Possible Thermal Impact
- Auto-halt (max)	1.0W @ 166 MHz	0.71W @ 266 MHz	
- Stopclk (max)	50mW	62mW @ 266 MHz	
o Signal Levels (inc'l clocks)	3.3V	2.5V	"New" Clock Design L2 Cache [PBSRAM]
o Bus:Core Ratio		2/7 & 1/4 ratio added	Extended product offering
o Pinout		BF2, PICD0-1, PICCLK pins added	Layout Change
o CPUID	04H	08H	BIOS Change
o Packaging	TCP/PPGA	TCP/Mobile Module	Package Migration
o Die Size	DL=12.855 mm DW=11.105 mm	DL=10.450 mm DW=9.088 mm	Re-qual Thermals & Die Attach
o Process Technology	0.35 um	0.25 um	Lower Vcc/Power Dissipation

Vcc2/Vcc3 Voltage Supply

- **Vcc Specs**

	Min Voltage	Max Voltage	Tolerance
Vcc3	2.375V	2.625V	2.5V +/- 0.125V
Vcc2	1.665V 1.850V	1.935V 2.150V	1.8V +/- 0.135V (166-233 MHz) 2.0V +/- 0.150V (266 MHz)

- **Sequencing**
  - No specific sequence required for the Mobile PPMT on 0.25 Micron CPU
  - It is recommended that Vcc2 and Vcc3 power supplies be either both ON or both OFF within 1 second of each other.
  - Other platform elements (such as chipset, SRAM,...) may require a specific dual supply voltage sequence; consult vendor specifications
  - 430TX has a specific sequence; consult specification

- **Keep power supply design flexible to accommodate processor requirements**
  - Vcc2 should be able to adjust between 1.8 and 2.0V
  - Vcc2 should be adjustable independent of Vcc3

Capacitive Decoupling

- **Bulk Cap Recommendations (assumes 0.1 Ohm ESR caps)**
  - 166/66 MHz: (Vcc_core = 1.8V +/- 0.135V)
    - Vcc2: 2x 100uF, 2x 220uF Tantalums with 300KHz switching regulator
    - Vcc3: 1x 33uF
  - 200/66 MHz: (Vcc_core = 1.8V +/- 0.135V)
    - Vcc2: 2x 100uF, 2x 220uF Tantalums with 300KHz switching regulator
    - Vcc3: 1x 33uF
  - 233/66 MHz: (Vcc_core = 1.8V +/- 0.135V)
    - Vcc2: 3x 100uF, 2x 220uF Tantalums with 300KHz switching regulator
    - Vcc3: 1x 47uF
  - 266/66 MHz: (Vcc_core = 2.0V +/- 0.150V)
    - Vcc2: 7x 220uF (or 5x 220uF/ESR=0.07 Ohms) Tantalums with 300KHz switching regulator
    - Vcc3: 1x 100uF
- **High Frequency Decoupling**
  - Use multiple 0.1uF and 0.01uF bypass caps
- **Capacitive decoupling must be verified for each design to guarantee Vcc spec compliance**
  - Designing in margin today will avoid redesigns for future processors
  - Excel* Worksheet available to help assess your CPU decoupling cap values
- **Consult with your power supply vendor for the exact values of decoupling needed for specific designs**

Thermal Design Power Definitions

- **Thermal Design Power (Max)**
  - Usage - This value should be used for system thermal design. Systems must be designed to thermally dissipate this level of power as a steady state condition while keeping the CPU temperature in spec.
  - Definition - Maximum power dissipation under normal operating conditions (no pins shorted together, etc.) at nominal Vcc, worst case temperature, while executing the worst case power instruction mix.
- **Thermal Design Power (Typical)**
  - Usage - This value can be used for system thermal design. System thermal design may either meet the thermal design maximum spec or provide a thermal feedback fail safe mechanism in case CPU power consumption exceeds the thermal design typical spec for prolonged periods.
  - Definition - Power dissipation based on the average and peak power of real applications under normal operating conditions (no pins shorted together, etc.) at nominal Vcc and room temperature.

Thermal Design Power

- **Thermal design also needs to be flexible to handle Vcc2 requirements**

Frequency	166MHz	200MHz	233MHz	266MHz
Vcc2	1.8V	1.8V	1.8V	2.0V
Vcc3	2.5V	2.5V	2.5V	2.5V
TDP max	4.1W	5.0W	5.5W	7.6W
TDP typ	2.9W	3.4W	3.9W	5.3W

- **All TDP numbers are validated with silicon**

Thermal Design Considerations

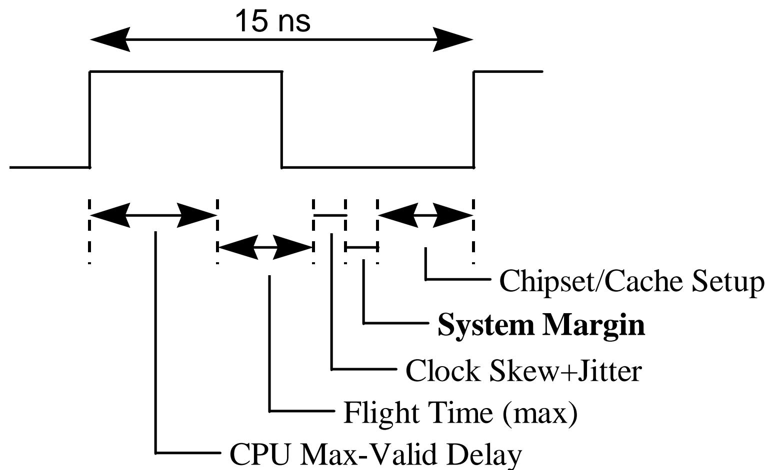
- **Specification Summary**
  - Thermal resistance
    - TCP Theta JC without enhancements = 0.8 deg. C/W
  - Max Tcase
    - 95C for TCP
- **Measure processor power when measuring thermals**
  - Will help calibrate Mobile PPMT on 0.25 Micron power vs. OEM's existing CPU designs (P55CLM, P54CSLM, or P54LM)
  - NB CPU Power Measurement Method and Thermal Implications white paper available to assist in determing thermal performance
- **Thermal design for TDP (typ)**
  - Disable Power Management while running thermal tests
  - Run application
    - Prime95
    - DEP
  - Conduct the test for at least 3 hours
  - Ensure that rest of the system component temperatures are within component specs
    - HDD, FDD, CD-ROM, SRAM, chipset etc.
- **Maximize Tcase margin for possible future processors**
  - Will save future rework

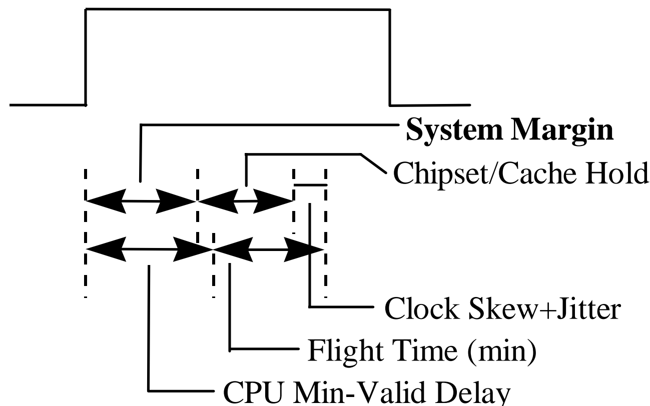
I/O Signals

- **All I/O signals are 2.5V tolerant only (not 3.3V)**
- **Clock Levels**
  - CLK, PICCLK, TCK require 2.5V signals
  - Clock buffers are not 3.3V tolerant
  - Refer to CKDM-66M Specifications (Version 1.1, doc#: SC 2063)
- **Clock Undershoot/Overshoot specifications**
  - Refer to Mobile PPMT on 0.25 Micron datasheets (Order number: 243468-001) page 53-54 (Table 21-22) for Overshoot/Undershoot specifications
  - Reduce as much as possible while still meeting rise/fall time
- **Timing Margins**
  - 66MHz AC bus timings slightly different between P55CLM and Mobile PPMT on 0.25 Micron
    - Min and Max Valid Delays affected
    - Vil max also affected
  - Design for maximum system timing margins
  - System timing margins are a function of CPU valid delays, clock skews, flight times, and chipset setup/hold times (see next slide)
  - Flight times minimization can be accomplished with:
    - Optimized layout design (minimizing trace lengths/routing, etc.)
    - I/O simulations using appropriate buffer models for CPU/chipset/SRAMs
    - I/O buffer modeling (available in EDS Rev. 2.0)
    - Linear IBIS modeling (available on request)

I/O Signals (Cont'd)

- **Timing Margins** (66MHz example)





- **CPU Max-Valid Delay**
  - CPU Max-VD increases
  - Flight time and Clock skew are approximately constant
  - Chipset/cache setup times and system margin stressed

System Margin = 15 - (CPU Max-VD + Flt time + Clk skew + Chipset setup)

- **CPU Min-Valid Delay**
  - CPU Min-VD decreases
  - Flight time and Clock skew are approximately constant
  - Chipset/cache hold times and system margin stressed

System Margin = (CPU Min-VD + Flt time) - (Clk skew + Chipset hold)

I/O Signals (Cont'd)

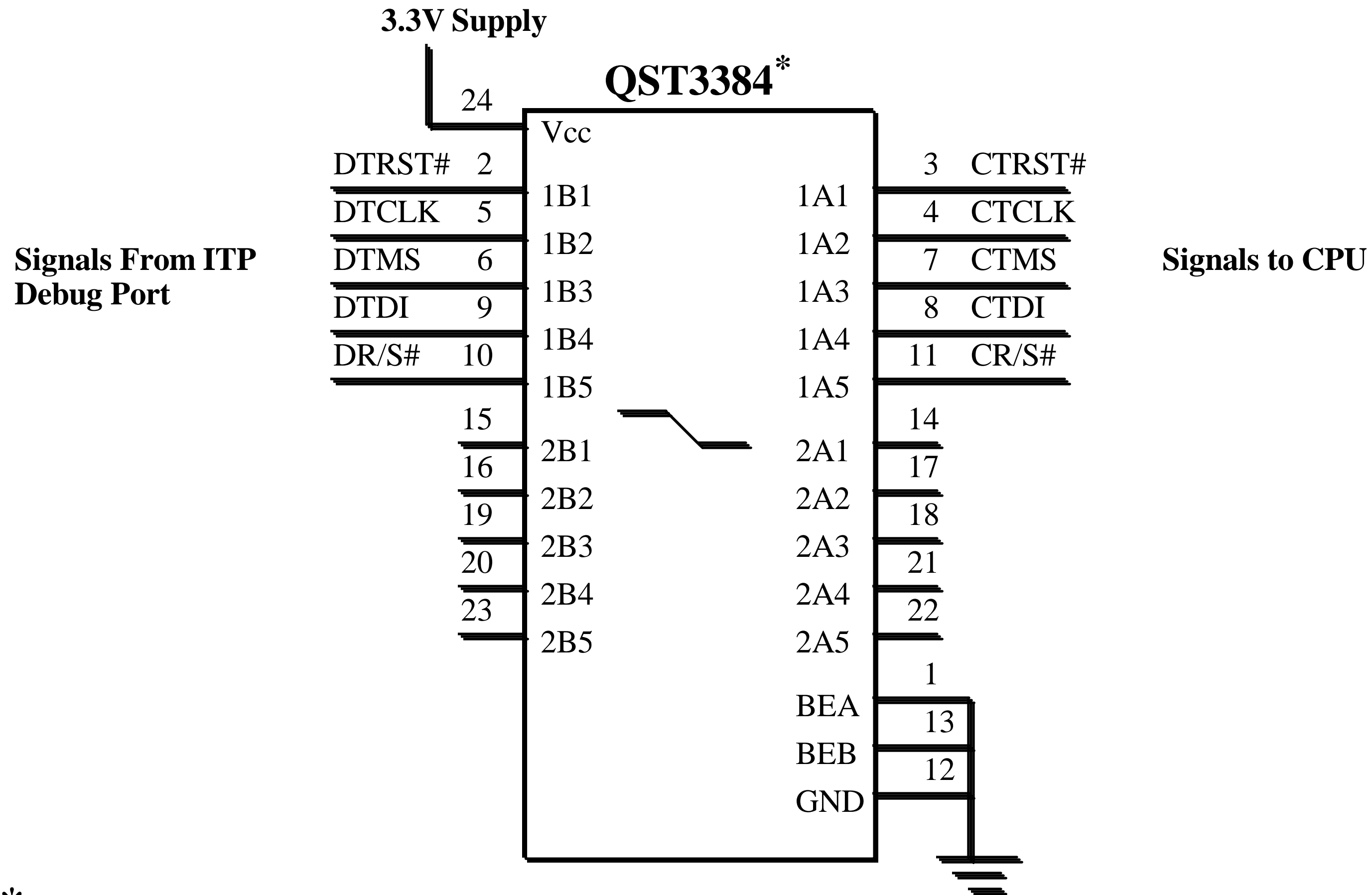
- **Vil (max) Change**
  - Due to reduced Vcc, $V_{IL\ max} = 0.5V$
  - SRAMs spec'd to handle lower Vil (max); ($V_{OL,\ max}$ spec = 0.2V)
  - OEMs need to validate SRAMs meet CPU signal level requirements
  - Signals requiring external pullups may be affected
    - Use of large pullups is recommended to maintain sufficient noise margin
    - Signals affected are for configuration only (e.g.,BRDY#, BUSCHK#)

I/O Signals (Cont'd)

- **ITP/JTAG Interface requires existing 3.3V debug equipment**
  - Q-switch can be used to interface 3.3V signals to Mobile PPMT on 0.25 Micron JTAG interface (TRST#, TCLK, TMS, TDI, R/S#)
  - National, Quality Semiconductor, and TI have suitable Q-switches
  - CPU 'piggy back' board may be inserted between ITP debug port cable and board connector
    - 3.3V needs to be supplied to 'piggy back' board
    - OEM may choose to implement Q-switch circuit in his board design to eliminate 'piggy back' board

ITP/JTAG Interfacing Example

- **3.3V must be supplied to Q - switch**



Bus-to-Core Ratio Changes

- **BF2 pin added for possible future upgrades**
  - Default = 0
  - Layout option to allow possible future external pull-up to 2.5V

BF2** (pin 184)	BF1 (pin 185)	BF0 (pin 186)	Mobile PPMT on 0.25 Micron	P55C	Mobile PPMT on 0.25 Micron Freq
0	0	0	2/5	2/5	166/66MHz
0	0	1	1/3	1/3	200/66MHz
0	1	0	1/2*	1/2*	
0	1	1	2/7	Reserved	233/66MHz
1	0	0	1/4	N/A	266/66MHz

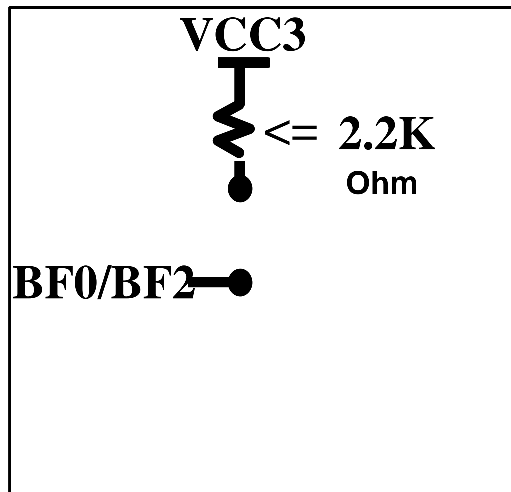
* Note that the Mobile PPMT on 0.25 Micron defaults to the 1/2 bus-to-core ratio
** BF2 is not defined for P55CLM

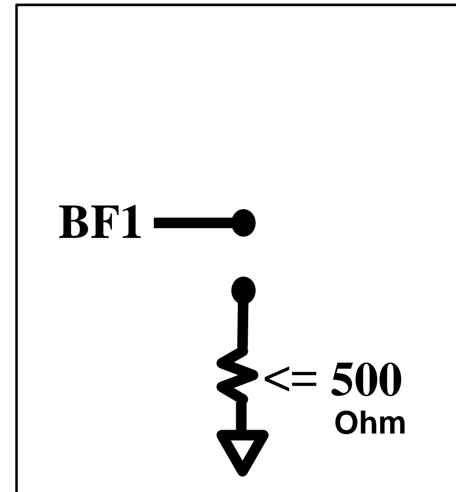
- **External pull-up/pull-down resistor values for BF0, BF1, and BF2**

Pin Name	External Resistor Type	Recommended Value (ohm)
BF0/BF2	pull-up	< 2.2K
BF1	pull-down	< 500

Bus-to-Core Ratio Changes (cont'd)

- **For maximum flexibility, jumpers should be used to configure BF0-2**





I/O Signals (cont'd)

- **Input pins must be connected to Vss if not used by the system**
  - AHOLD, KEN#, WB/WT#, NA#, INV, BRDY#, or EWBE#
  - If not driven by system logic must be tied to ground via a weak pulldown resistor (i.e. >2 Kohms)

Processor CPU ID

- **Mobile Pentium(R) Processor with MMX™ Technology on 0.25 Micron CPUID is new** (Different from P55CLM)
  - Mobile PPMT on 0.25 Micron uses a model number of 08H; P55C used 04H
  - BIOS/application code that uses model number may need to change
  - Feature register may be accessed to determine specific features such as support for MMX™ technology

CPUID	Reserved [31:14]	Type [13:12]	Family [11:8]	Model [7:4]	Stepping [3:0]
Mobile PPMT on 0.25 Micron	0	0h	5h	**8h**	x
P55CLM	0	0h	5h	4h	x
P54CSLM	0	0h	5h	2h	x

Packaging

- **Mobile PPMT on 0.25 Micron -166, 200, 233, & 266 available in TCP and Mobile Module packaging**
- **Die Size**
  - Production die-size (0.25 micron) smaller than P55CLM (0.35 micron)
    - May require adjustment in the die-attach process

Product	**Die Length (DL)**	**Die Width (DW)**
P55CLM	**12.855 mm**	**11.105 mm**
Mobile PPMT on 0.25 Micron	**10.450 mm**	**9.088 mm**

Pin#11(BRDYC#) and Pin#190 (FRCMC#) Connection Issue

Design Consideration for Mobile Pentium(R) Processor with MMX(TM) Technology on .25 Micron only:

Pin#11 (Vcc2) and pin#190 (Vcc2) on the Mobile Pentium Processor with MMX Technology on .25 Micron can be connected to either Vcc2 or Vcc3.

When connected to Vcc2, there is a minor increase in leakage current (up to 300uA) on pin#11 and pin#190. To avoid the incremental leakage current, those pins are recommended to connect to Vcc3.

pin#11 and pin#190 should be tied to Vcc3 to design for maximum margin in Vih spec. For future low power offerings of Mobile Pentium Processor with MMX Technology on .25 Micron, it is recommended to connect to Vcc3.

Key Platform Validatation Areas

- **Validation of O/S legacy applications and MMX(TM) applications**
- **2.5V I/O interface signal integrity**
  - Clock signals meet 2.5V spec
  - SRAMs/chipset signals meet interface spec (especially CPU Vil = 0.5V)
- **System tuning - flight time measurements and AC timing margin analyses**
- **Voltage supply solution**
- **System thermal solution**
- **CPU stress testing**

Due to Mobile PPMT on 0.25 Micron operating characteristics, several validation areas need to be emphasized

Platform Readiness/Checklist Summary

- **Clock chip compatibility verified**
  - Clock levels measured and within 2.5V spec
  - Undershoot/Overshoot/Rise/Fall within specification
- **SRAM/chipset compatibility verified**
  - Voh/Vol measured and within Vil/Vih CPU spec
- **Chipset AC timing compatibility verified**
  - Flight time measurements made and sufficient AC timing margin verified
- **Power supply compatibility verified**
  - Tolerance measurements made and within spec
    - Transient noise within budget
    - Hi-frequency noise within budget
- **Thermal design capable of handling CPU/system requirements**
  - Tcase, Tamb, and power measured using worse case applications

Mobile Pentium(R) Processor With MMX(TM) Technology On 0.25 Micron Collaterals

Document	Date
Mobile PPMT on 0.25 Micron Platform Architecture Analysis Rev. 1.0	**Now**
CPU Power Measurement Method and Thermal Implications	**Now**
EDS Rev 2.0	**Now**
Mobile Design Considerations Rev. 2.0	**Now**
IBIS Model	**Now**
BSDL File	**Now**
Mobile PPMT on 0.25 Micron 200/233 MHz data sheets	**Now**
Mobile PPMT on 0.25 Micron 166/266 MHz final specs	**Now**
Mobile PPMT on 0.25 Micron 166/266 MHz data sheets	**Now**
Mobile PPMT on 0.25 Micron performance brief (166-266 MHz)	**Now**