

TL/G/10035-46

DESCRIPTION

Process 94 is a monolithic dual JFET. It is strictly intended for operational amplifier input buffer applications. Special processing results in extremely low input bias current and virtually unmeasurable offset current. It is important to note that the <5 pA bias current is measured at 35V. Typical CMRR is 125 dB. Performance superior to electrometer tubes can be readily achieved with low offset voltage and almost zero long term drift.

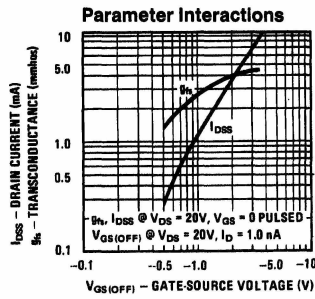
Electrical Characteristics ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{GSS}	Gate-Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1 \mu A$	-40	-70		V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 15V, V_{GS} = 0V$	0.5	3.0	10	mA
g_{fs}	Forward Transconductance	$V_{DS} = 15V, V_{GS} = 0V$	1.5	3.5	7.0	mmho
g_{fs}	Forward Transconductance	$V_{DG} = 15V, I_D = 0.2 \text{ mA}$	0.7	1.2	1.8	mmhos
$V_{GS(OFF)}$	Pinch Off Voltage	$V_{DS} = 15V, I_D = 1 \text{ nA}$	-0.5	-2.0	-6.0	V
I_G	Gate Current	$V_{DG} = 35V, I_D = 0.20 \text{ mA}$		2.0	15	pA
C_{rss}	Feedback Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1 \text{ MHz}$		0.01	0.02	pF
C_{iss}	Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1 \text{ MHz}$		4.0	5.0	pF
e_n	Noise Voltage	$V_{DG} = 15V, I_D = 0.2 \text{ mA}, f = 10 \text{ Hz}$		12	50	nV/\sqrt{Hz}
g_{os}	Output Conductance	$V_{DG} = 15V, I_D = 0.2 \text{ mA}$		<0.1		μmhos
$ V_{GS1} - V_{GS2} $	Differential Match	$V_{DG} = 15V, I_D = 0.2 \text{ mA}$		5.0	25	mV
$\Delta V_{GS1} - V_{GS2}$	Differential Match Drift	$V_{DG} = 15V, I_D = 0.2 \text{ mA}$		6.0	50	$\mu V/^\circ\text{C}$
CMRR	Common-Mode Rejection	$V_{DG} = 15V, I_D = 0.2 \text{ mA}$		125		dB

This process is available in the following device types. *Denotes preferred parts.

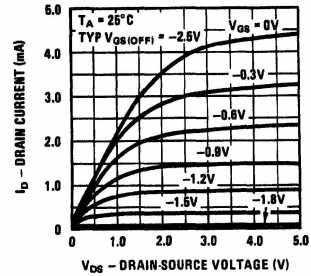
TO-71 (NS Package 12)

- *NDF9406
- *NDF9407
- *NDF9408
- *NDF9409
- *NDF9410



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Common Drain-Source Characteristics



TL/G/10035-48

